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# Dual-Purpose Star Tracker and Space Debris Detector: Miniature Instrument for Small Satellites

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## Abstract

This paper presents the conception, design and real miniature instrument implementation of a dual-purpose sensor for small satellites that can act as a star tracker and space debris detector. In the previous research work, the authors conceived, designed and implemented a breadboard consisting of a computer laptop, a camera interface and camera controller, an image sensor, an optics system, a temperature sensor and a temperature controller. It showed that the instrument was feasible. In this paper, a new real star tracker miniature instrument is designed, physically realized and tested. The implementation follows a New Space approach; it is made with Commercial Off-the-Shelf (COTS) components with space heritage. The instrument's development, implementation and testing are presented.

**Keywords:** miniature instrument; star tracker sensor; space debris detector; small satellites; image sensor; microprocessor; architecture; parallel interface



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## 1. Introduction

One of the key aspects contributing to the success of a space mission is attitude determination, which has to be reliable and accurate. This is achieved by using star trackers (STRs) [1]. STRs are optical devices that determine the satellite attitude by detecting the stars in its Field-of-View (FoV). The equipment comprises an optical system, an image sensor and an onboard computer [2–8].

Since this is an ongoing work of our research group [6–8], the state of the art of this paper is focused on the two main components of the STR miniature instrument, i.e., the microprocessor or Data Processing Unit and the image sensor.

The authors from [9] developed an STR using an AMD 486 processor as the Data Processing Unit; the specifications of the processor included 4 MB of RAM, a 4 MB Flash Disk and support circuitry. The Flash Disk contained all necessary programs, data and star catalogs. The Data Processing Unit communicated with the user via an RS422 serial link. Using a flash memory for program storage allowed for remote updates to be provided to all software via the RS422 link. As the RS422 utilized balanced drives, the cable between the Data Processing Unit and the control computer may have been several hundred meters in length. The power consumption of the Data Processing Unit was 7.5 W (including that required to operate two camera head units) running on a 28 V power supply.

The hardware used for the Sharp Edge Flight EXperiment (SHEFEX) 2 star tracker includes a suitable Charge-Coupled Device (CCD) camera with a corresponding lens and a PC/104 computer for the image processing chain [10,11]. All equipment has to demonstrate its acceptance and qualification levels for operation in space [10,11].

The SHEFEX 2 experiment aims to select a Commercial Off-the-Shelf (COTS) camera, giving the best images at a reasonable price. With this objective, it is clear that only sensors with limited sensitivity can be chosen. This leads to a reduced number of stars that can be detected. The need arises to select a lens that gives a wide FoV in order to detect enough stars in one image. Furthermore, the unwanted limitation of image smear is responsible for the short-required exposure times while still needing to maintain a maximum signal-to-noise ratio (SNR) [10].

Based on several indoor and night sky tests, it was decided to use the monochromatic CCD camera (Atik Cameras Unipessoal Lda., Lisbon, Portugal) (model: PROSILICA EC655). The lens used for the star tracker camera was a PENTAX 25 mm lens with manually adjustable focus and brightness. The FoV obtained with this lens is 14.87 deg $\times$ 11.15 deg, which results in a diagonal FoV of 18.57 deg [10].

The company Jena-Optronik GmbH (Jena, Germany) has a long heritage in star tracker design. The first activities in this field started in the early 1980s and resulted in the first launch worldwide of a fully autonomous star tracker system, ASTRO1, to the Russian MIR space station in 1989. In the following years, the ASTRO star tracker family was continuously improved and enlarged [12]. The processor used was a high-performance radiation-hardened SPARC V8 architecture of type AT697E, which was implemented with full triple-modular redundancy, error detection and correction (EDAC) and parity protection, ensuring excellent performance under harsh environmental conditions. This system solved the loss in space condition in just 1 sec (attitude acquisition without a priori knowledge) [12].

In [5], the authors present the design, simulation and implementation of an STR for Low Earth Orbit (LEO) satellites. An MT9P031 complementary metal–oxide–semiconductor (CMOS) image sensor from Aptina Imaging (San Jose, CA, USA) was used to capture image data. The STR uses a Texas Instrument OMAP3530 ARM Cortex A8 processor (Dallas, TX, USA). This processor supports powerful graphic interfaces, reducing the size and power consumption. For storage and processing, the STR uses a NAND flash memory. For the communication interface to the satellite, a CAN Bus is used.

Reference [13] reports a nano-star tracker based on a CMOS image sensor. This nano-star tracker is a miniaturized, low-power instrument that can be used for the precise attitude measurement of a satellite extension boom.

The studies conducted in the literature [5,9,10,12,14] all propose similar approaches to star tracker design, but our approach takes this a step further by presenting the conception, design and implementation of the avionics of a real miniature instrument for small satellites and the testing of a star tracker for space surveillance. Moreover, the advent of New Space enabled the use of COTS devices, with proven space heritage, for the microprocessor or

Data Processing Unit and the image sensor in order to reduce the size and costs of space-related equipment. In this context, this work proposes the development of a miniature instrument, i.e., a low-cost STR using COTS devices, focusing on the hardware design, implementation and tests. Since there is a lack of information in the literature on the hardware conception of an STR, this work contributes in demonstrating how to build an STR addressed for CubeSats and small satellites, i.e., selecting the best components, designing the most viable solution, implementing the solution and testing the STR.

This paper has the following structure: Section 2: Previous Research; Section 3: Optical Imaging System Conception and Design; Section 4: STR Breadboard Layout Design; Section 5: STR Implementation; Section 6: STR Tests and Results and Section 7: Conclusions.

## 2. Previous Research

In the previous research work that started in 2020 between Synopsis Planet, Universidade de Lisboa, Lisbon and Universidade de Coimbra, Coimbra, Portugal, the authors conceived, designed and implemented an STR breadboard consisting of a computer laptop, a camera interface and camera controller, an image sensor, an optics system, a temperature sensor and a temperature controller [6,8]. The temperature controller is connected to an external power supply and the computer. This device sends a programmed temperature to the thermoelectric cooler, cooling the aluminum pieces and, consequently, the optical sensor. The temperature sensor measures the temperature of the CMOS sensor. For more information, refer to [6], as it is an important complement to the current paper. The architecture of the previous star tracker is shown in Figure 1. The arrows connecting the blocks are to indicate that the information is bidirectional.

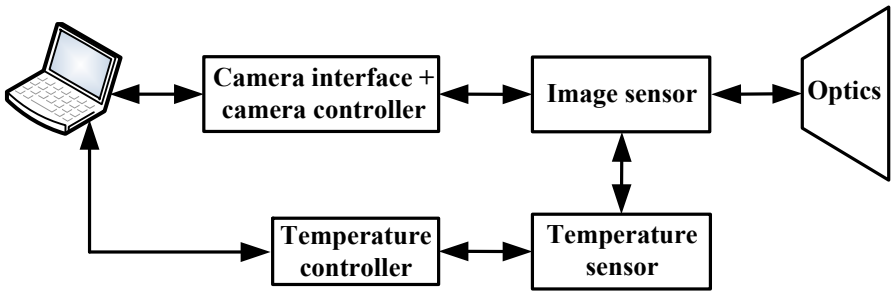



**Figure 1.** Architecture of the previous star tracker breadboard.

The previous STR breadboard was developed using COTS devices, and the components were selected based on the characteristics found in the literature. The breadboard's capability was tested by capturing night sky images [6].

Using the observation data from the previous star tracker breadboard, the authors evaluate the star tracking and space debris algorithms to be implemented in the payload camera [7]. For star identification and, consequently, attitude extraction, the authors chose the algorithm Tetra. The results were compared to the standard star identification software, Astrometry.net, to assess the attitude accuracy. Tetra is light and fast, and demonstrates a good performance with uncertainties of a few dozen arcsecs. For space debris detection, ASTRiDE and the developed Hybrid Time-Index image algorithms were used. The results were compared to establish a performance evaluation metric in terms of detectability, time and computational cost. Although the Hybrid algorithm is more powerful, it is also time-consuming, making ASTRiDE the better choice for an onboard computer [6,15–18].

The algorithm Tetra selects four neighbor stars and divides their distances by the brightest star from this group, storing the result in an array format. Then each array is compared to the internal catalog to match the stars and provide the spacecraft attitude. Tetra uses the minimum number of database accesses possible, in most cases, precisely one,

to reduce the computational time [7]. Astrometry.net takes as the input an astronomical image and provides the scale and the orientation of that image. The algorithm identifies the astronomic sources in the image, then divides the detected stars into groups of four and computes the relative position of each star inside a group. The algorithm then matches these stars with the internal catalog, providing information about the image's location, scale and orientation in the sky [7]. ASTRiDE is a different method to the previous ones due to the streak detection by each object's border and morphological parameters. The border is recognized using the boundary tracing method, which is a technique used to identify pixels in the boundary of an object. Then, the algorithm quantifies the shape of each border to distinguish streaks from other objects [7]. The Time-Index algorithm is divided into three parts: (i) image processing, wherein the non-uniform background, hot pixels (abnormally bright pixels) and flicker noise (an electronic noise that is a function of frequency) are removed from the image using a mean filter; (ii) Time-Index filtering, in which the stars and noise are extracted; and (iii) streak detection, wherein the streak is detected using the Time-Index multistage quasi-hypothesis-testing method [7].

## 3. Optical Imaging System Conception and Design

Based on the previous research (Section 2) and the conception of the general architecture of the optical imaging system (Figure 1), the authors proceed with the design of the electronic conception of the STR breadboard to meet the following five requirements:

(1) Power management block: responsible for switching and controlling the power draw of the system;
(2) Flash memory block: the primary memory storage for the system; it can be a Secure Digital (SD) card or an embedded MultiMediaCard (eMMC) chip;
(3) Sensor block: composed of the CMOS sensor, the power supply management of the sensor and parallel and series communication interfaces;
(4) Processor block: composed of the central processing unit (CPU) and the auxiliary components required to run the algorithms and perform image processing;
(5) Outwards communications block: set for different protocols and interfaces to communicate with the onboard computer system (OBCS) of the system via CAN-BUS, I2C and Ethernet.

The conception of the general architecture of the STR breadboard is shown in Figure 2.

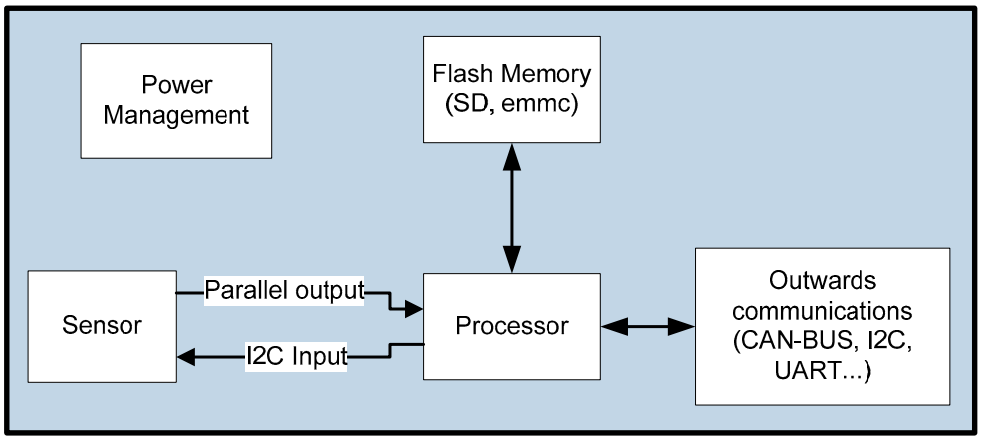



**Figure 2.** Conception of the general architecture of the optical imaging system breadboard.

Based on the general architecture of the optical imaging system breadboard (Figure 2), the next step is the selection of critical components with proven space heritage. An optical imaging system's performance is fundamentally reliant on two key components: the sensor

and the processor. The sensor is responsible for capturing images of the night sky, while the processor analyzes the images' data to identify stars and determine the system's orientation. These two components work in unison to ensure precise and reliable tracking.

The following subsections elaborate on why these two critical components (processor or Data Processing Unit and image sensor) with proven space heritage are the most important in the design of a star tracker. Additionally, they outline the various sensor and processor options that were considered during development, along with the rationale behind the final selections.

### *3.1. Image Sensor*

The image sensor (sensor block, Figure 2) is an important component of an STR. It must have enough resolution to provide accurate data, behaving as a stable, useful interface for the command and data transfer processes.

State-of-the-art STRs suggest [2–12,14] some relevant characteristics for the selection of image sensors for star tracking applications, detailed as follows:

- A CMOS is preferable to a Charge-Coupled Device (CCD).
- The pixel size should be between 2 μm and 6 μm, with the optimal pixel size being in the 4 μm to 6 μm range. A larger pixel size increases the sensor's sensitivity.
- A higher resolution increases accuracy but requires larger power consumption, memory and computational capacity. Moreover, it can induce the identification of false alarms by the algorithm. The minimal desired resolution is 512 pixels × 512 pixels.
- The image sensor must have a minimal SNR between 5 to 8.
- The image sensor should have a maximum power consumption of 500 mW.
- The image sensor must be capable of operating in the harsh environment of space. Thus, the sensor must mainly resist space radiation and must operate across a wide range of temperatures.

The image sensor for the star tracker is a CMOS and not a CCD, with the former being the preferred choice due to its advantages. Comparing between a CMOS and CCD, according to our experience, the CMOS is compact and has high reliability, extensive integration, a wide dynamic range and radio resistance, while the CCD has poor substantial volume, high power consumption and low space radiation resistance.

### *3.2. Processor*

The processor block (Figure 2), composed of the CPU, microcontrollers and field-programmable gate arrays (FPGAs) of CubeSats can be used as the processor of the star tracker. FPGAs have a successful legacy in space and continue to be implemented in space applications due to on-chip memory and power performance. Microcontrollers with ARM Cortex-A8 and ARM Cortex-A9 processors have also been successfully implemented in space, being used as the OBCS of CubeSats and star tracker processors [19].

Despite the usage and good performance of microcontrollers and field-programmable gate arrays (FPGAs), more simplified options are also evaluated for star trackers, for instance, open-source platforms. A wide variety of open-source platforms are promising for space applications, such as Arduino, BeagleBone, Raspberry Pi and Intel Edison. Each platform has a different processor, but all have demonstrated good results for imaging applications.

The processor ARM Cortex-A8 was selected for use in the STR due to its highly integrated, reliable and space-proven design, which simplifies the electronics complexity while providing excellent power efficiency, real-time processing capabilities and a wide operational thermal range. Additionally, our research group already has experience in pro-

gramming processors of this family. The processor ARM Cortex-A8 has been successfully tested up to 8 krads.

## 4. STR Breadboard Layout Design

The design layout blocks of the STR breadboard are shown in Figure 3.

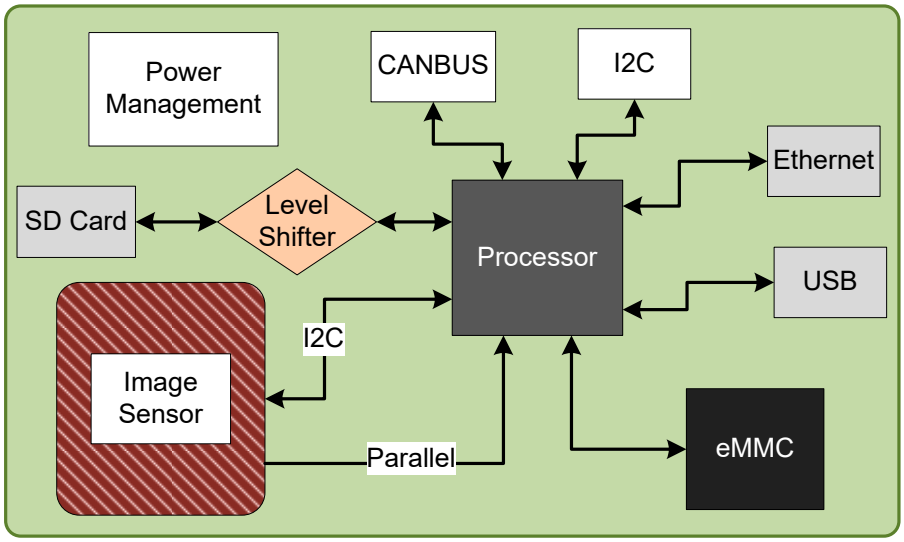



**Figure 3.** Design layout of the STR breadboard.

The layout of the STR breadboard was chosen to make the routing more direct, as shown in Figure 3. The sensor pins are located to the left of the CPU (processor), while the Ethernet and USB pins are located to the right. The eMMC (flash memory block) is located at the bottom, and the CAN-bus and I2C (outwards communications block) are located at the top. The SD card is located to the left of the CPU and has a level shifter to convert the voltage to the required level.

The Power Management block includes the Power Management Unit (PMU), which is independent of the CPU as it only monitors the power drawn by the board and has no logical connection to anything else. The power management block architecture of the image sensor system is shown in Figure 4.

In Figure 4, the supply voltage to the PMU block varies between +5 V and +15 V. In the PMU, the supply voltage is converted into a stable +5 V, which serves as the system's primary operating voltage. A current limiter (1 A) sub-block is incorporated to prevent short circuits and to control power consumption within designated limits.

Two voltage monitors are utilized to detect potential voltage leaks—one for the main 5 V power supply to the processor and another one for the 1.8 V secondary power source used by the I/Os.

Dedicated voltage regulator sub-blocks are used for the Ethernet driver to ensure the required power levels are met. Additionally, voltage regulators are included for the image sensor, which can be selectively turned on or off to optimize energy consumption according to system requirements.

The image sensor breadboard and the processor breadboard were designed in Altium Designer on a two-layer printed circuit board (PCB) for a lead-less chip carrier (LCC) package and a four-layer PCB for a ball grid array (BGA) package which was later manufactured by the company Sinuta based in Aveiro, Portugal.

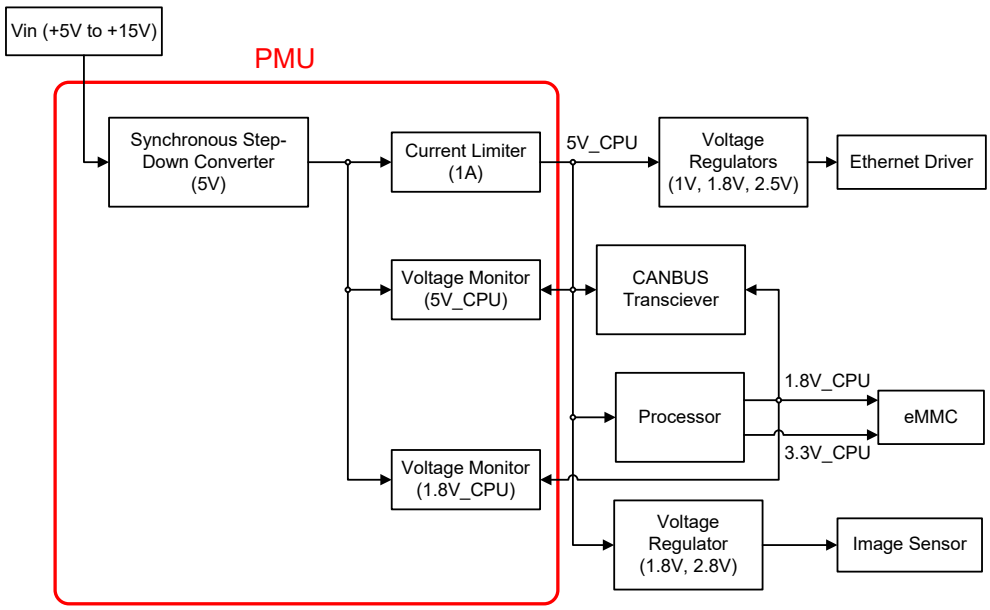
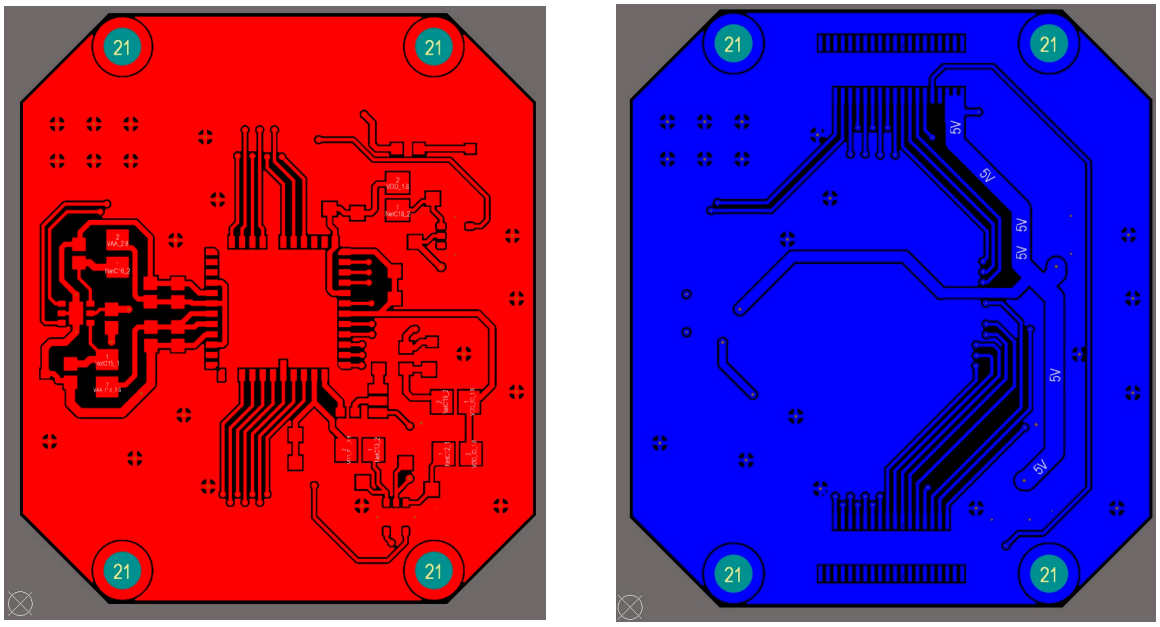



**Figure 4.** Power management block architecture of the image sensor.

### *4.1. Image Sensor Breadboard Layout*

The image sensor captures images of stars and space debris in the sky and is capable of transmitting the resulting data to the microprocessor through a 12-bit parallel output port. The sensor can function in either video (master) mode or frame trigger mode. Furthermore, it is controlled by the microprocessor via an I2C bus, facilitating the configuration of essential parameters such as resolution, exposure time, digital gain and frame rate. The image sensor breadboard layout designed in Altium Designer is shown in Figure 5.




(**a**) PCB layout top layer (**b**) PCB layout bottom layer

**Figure 5.** Image sensor breadboard layout designed in Altium Designer on a two-layer board.

The breadboard is structured as a two-layer board, which is suitable given the sensor's simplicity and the relatively low frequency of the data signals (up to 74 MHz).

### 4.2. Processor Breadboard Layout

The processor breadboard provides sufficient space for integrating essential components while maintaining a compact footprint. The processor breadboard layout designed in Altium Designer is shown in Figure 6.

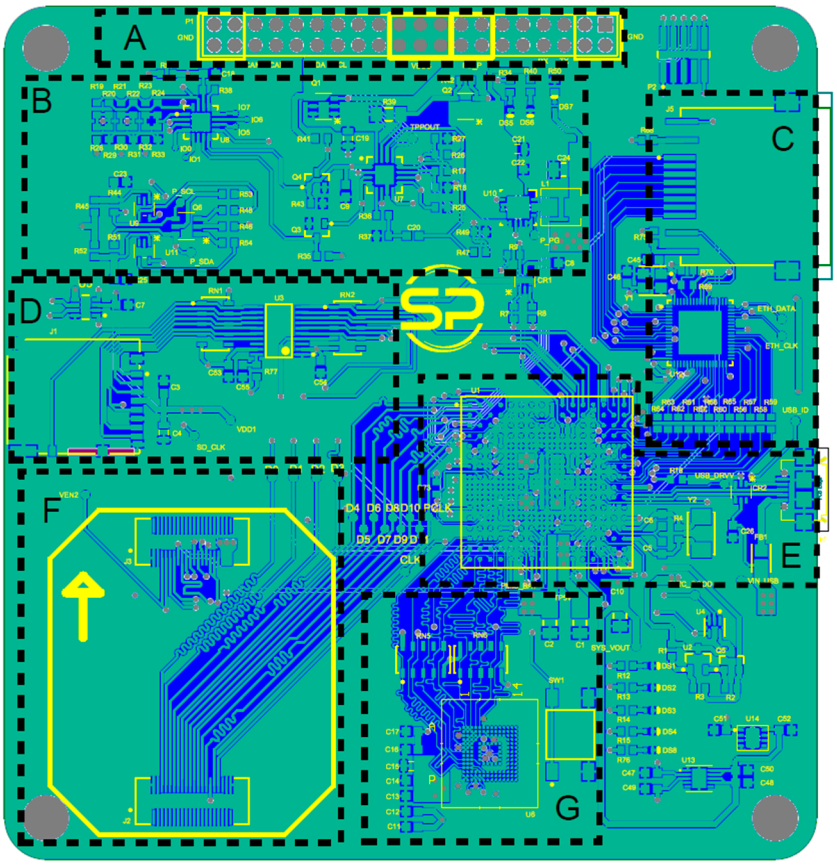



**Figure 6.** Processor breadboard layout designed in Altium Designer.

In Figure 6 the layout of the processor breadboard is divided into seven sectors, A to G (black font), as follows:

- A: This is a connector located in the top section of the PCB and acts as the primary power input interface, granting access to communication buses such as I2C, CAN Bus and UART for external peripherals.
- B: The PMU regulates power throughout the board. It features a switching voltage regulator that converts input voltages ranging from +5 V to +15 V down to a stable +5 V, along with two additional voltage regulators providing +5 V (primary) and +1.8 V (secondary) outputs. A 1 A current limiter is included for protection, and a timer circuit resets the power in the event of failure, thereby enhancing system reliability.
- C: An Ethernet driver and port to facilitate network communication, enable high-speed data transfers and allow for package updates for the STR.
- D: A micro SD card slot offers a memory expansion option and provides a convenient means for system debugging. By swapping different SD cards, users can test configurations and analyze data on a computer, streamlining the troubleshooting process.
- E: The core of the PCB contains the microprocessor and a USB connector, which is utilized for system debugging purposes.
- F: The bottom-left section features a dedicated connector for interfacing with the STR board, ensuring seamless integration between both systems.

- G: An eMMC storage module serves as a secondary memory option. After debugging, testing and configuring are completed, the eMMC is designed to be flashed with the same operating system as the SD card and to take its place in operation.

To integrate the image sensor with the processor PCBs, an integrated PCB was carefully designed in Altium Designer and the corresponding 3D model is shown in Figure 7.

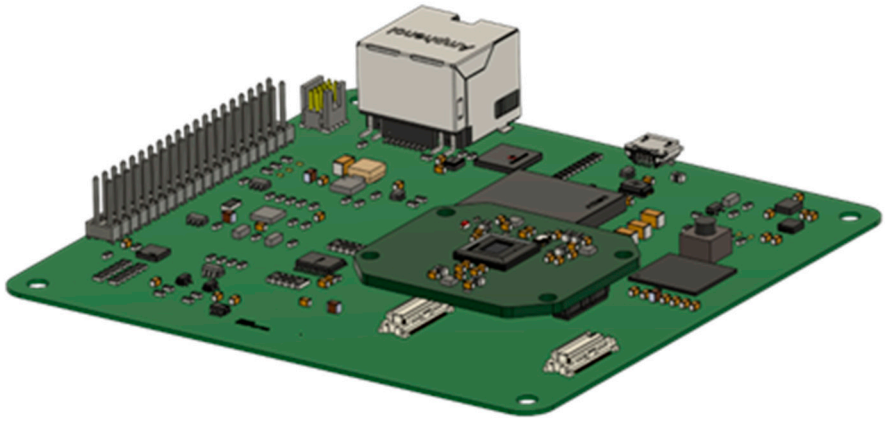


**Figure 7.** Three-dimensional model of the integrated image sensor and processor PCBs.

## 5. STR Implementation

The final assembly of the STR miniature instrument is shown in Figure 8.

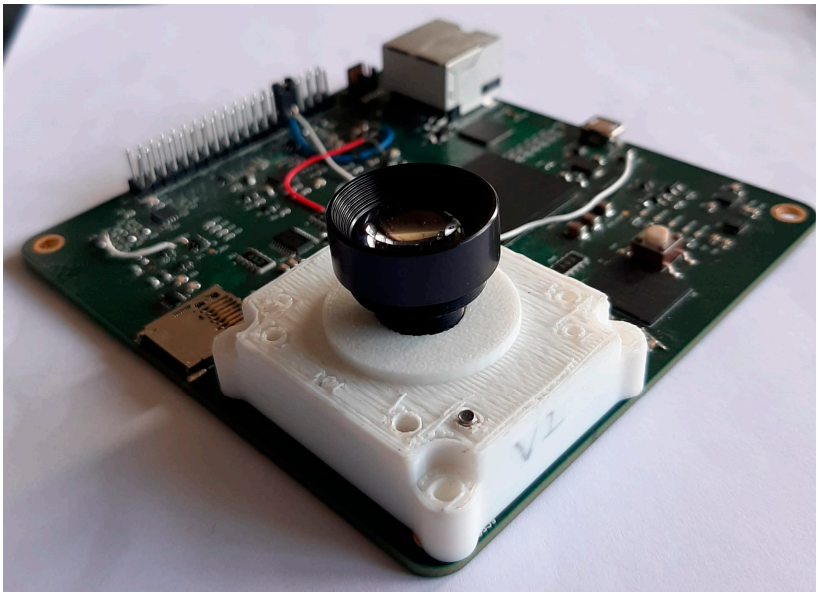


**Figure 8.** Final assembly of the STR miniature instrument.

Once the star tracker was fully assembled (Figure 8), the next step was implementing the software that configured and initialized the components, allowing for communication between the integrated PCBs. This process involved several key steps. First, the Electrically Erasable Programmable Read-Only Memory (EEPROM) was programmed. Next, the system was booted from an SD card by loading the PocketBeagle image and verifying startup.

The image sensor was then integrated, requiring the development of a custom device tree to support it. The Programmable Real-Time Units (PRUs) available on the processor were utilized, as they can capture high-speed data from each pixel and ensure synchroniza-

tion with the pixel clock. Finally, the complete operating system image was loaded onto the eMMC, ensuring that the system could boot and operate reliably from internal storage.

## 6. STR Tests and Results

After the star tracker was implemented and fully assembled and the software implemented, the next step was to debug and test each breadboard to ensure proper functionality. The debugging process included the following tests:

### *6.1. Image Sensor Tests*

The image sensor functioning test is conducted, wherein the clock lines (both External and Pixel), the I2C communication and the image signals of Line Frame and Frame Valid are checked. The clock line oscilloscope snapshot of the Pixel Clock (yellow trace) and External Clock (blue trace) are shown in Figure 9.

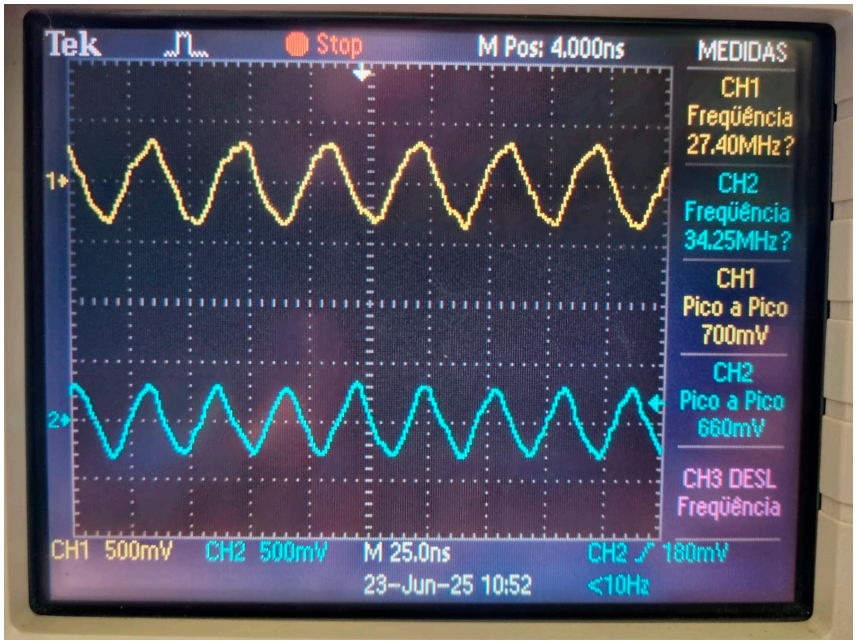



**Figure 9.** Clock line oscilloscope snapshot: Pixel Clock (yellow) and External Clock (blue).

Figure 9 shows the External Clock and Pixel Clock, 4.0 ns scale. The External Clock is crucial for the image sensor and operates using a 27 MHz oscillator crystal. This clock serves as the master clock, enabling the Phase-Locked Loop (PLL) to generate the Pixel Clock at the desired frequency, and facilitating software and I2C communication for configuration purposes. Thus, with communication debugging, there is confidence and satisfaction that both digital and analog signals are functioning as intended. The successful validation of these signals ensures robust signal integrity across the system, providing a reliable foundation for further development.

### *6.2. Power Consumption and Thermal Analysis*

The power consumption and thermal behavior of the STR are measured across different modes of operation. The values of thermal behavior are then used as inputs for a thermal analysis conducted in ESATAN-TMS [17], simulating the different scenarios and different modes of operation.

The different scenarios are as follows:

(a) The star tracker at a Sun exclusion angle of 18.5°;
(b) The star tracker pointing directly at the Sun;

(c) The star tracker operating in shadow, a cold case with all electronic components (EEEs) turned off.

The different operating modes are as follows:

(a) Boot mode: During this mode the OS is loaded to the CPU, installing every device tree and kernel module.
(b) Idle mode: In this mode, the processor is ON but no program is running. This is representative of the STR after booting and being ready to receive commands.
(c) Standby mode: In this mode, the sensor is ON and running, ready to take pictures.
(d) Video mode: This operating mode shows the power draw while capturing and displaying pictures continuously at 5 frames per second (fps).
(e) Space Debris mode: In this mode, the system captures an image and processes it through Tetra3 [16] followed by ASTRiDE [18]. There might be some deviations since the tests are performed in the lab without a real image to process.
(f) ASTRiDE mode: In this operating mode, the algorithm is executed with a test image from a database.
(g) Tetra3 mode: In this operating mode, the algorithm is executed with a test image from a database.

#### 6.2.1. Instrument Power Consumption

A series of tests were conducted to measure the power consumption of the STR under the different operating modes previously described using the setup shown in Figure 10.

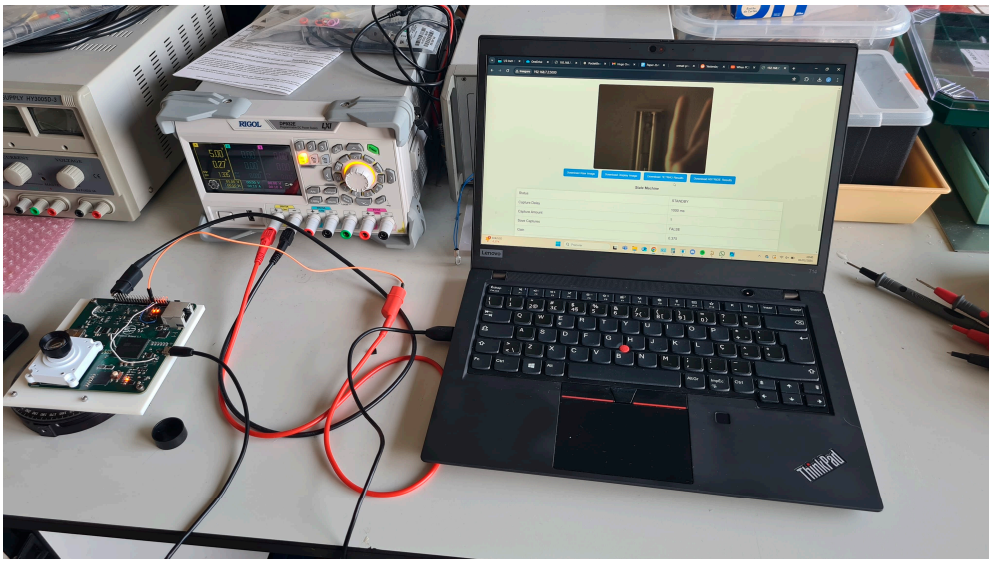



**Figure 10.** Setup for the power consumption measurement.

The different operating modes using the setup implemented in Figure 10 were executed multiple times to achieve an average of the power consumption while other modes (idle and standby) were run continuously. For capturing the data, a power supply was used Rigol DP932E (Suzhou, China) (details about the power supply can be found in [20]), which has data-logging capabilities. For these tests the voltage, current and power were extracted. The sample rate was 1 sample per second for all tests. The tests of power consumption per operating mode are presented in Table 1.

**Table 1.** Power consumption per operating mode.

| Operating Mode | Minimum (W) | Medium (W) | Maximum (W) |
|---|---|---|---|
| Boot | 0.57 | 1.18 | 1.96 |
| Idle | 0.60 | 0.61 | 1.16 |
| Standby | 0.83 | 0.98 | 1.70 |
| Video (5 fps) | 0.63 | 1.22 | 2.24 |
| Space Debris | 0.82 | 1.23 | 1.85 |
| ASTRiDE | 0.89 | 1.39 | 1.92 |
| TETRA3 | 0.60 | 1.08 | 1.87 |

The operating modes with the highest power consumption (Table 1) are the Video, Boot and ASTRiDE modes.

#### 6.2.2. Thermal Simulations

Using ESATAN-TMS software, version 2024 and following the power consumption measurements at different operational modes, thermal simulations were conducted [17] to assess the thermal behavior of the system under various environmental conditions. These simulations incorporate both conductive and radiative heat transfer mechanisms, ensuring a comprehensive evaluation of the thermal response in different operational and non-operational scenarios. The thermal results for the worst-case scenarios provide insight into the thermal constraints of the system, identifying potential risks of overheating or excessive cooling that could impact functionality.

In total, three worst-case scenarios were simulated for the STR: (i) Hot Operational Case (with STR at Sun exclusion angle of 18.5°), (ii) Hot Operational Case (with Solar irradiation directly falling on the image sensor) and (iii) Cold Non-Operational Case (with all electronics Off). All scenarios highlight key temperature distributions and their implications for system performance.

For the thermal cases (i) and (ii) above, the following characteristics/parameters are relevant:

(a) Nominal steady-state;
(b) Mechanical interface temperature: +40 °C;
(c) Ambient temperature: −270.15 °C;
(d) Sun positioned at 18.5° (Sun exclusion angle) from the central axis of the STR, OR Solar irradiation directly falling on the image sensor;
(e) The EEEs are operational (Space Debris mode).
(i) Hot Operational Case (with STR at a Sun exclusion angle of 18.5°)

The temperature map for the Hot Operational Case with the STR at a Sun exclusion angle value of 18.5° is shown in Figure 11.

In Figure 11, the temperature of the board ranges between 75.04 °C and 80.44 °C. The results indicate that electronics are operating near their maximum derated temperature limits, particularly at the junction level, where the derated limits typically range from 80 °C to 85 °C. While the board remains operational, it is close to exceeding safe margins, suggesting that thermal improvements may be necessary to ensure long-term reliability.

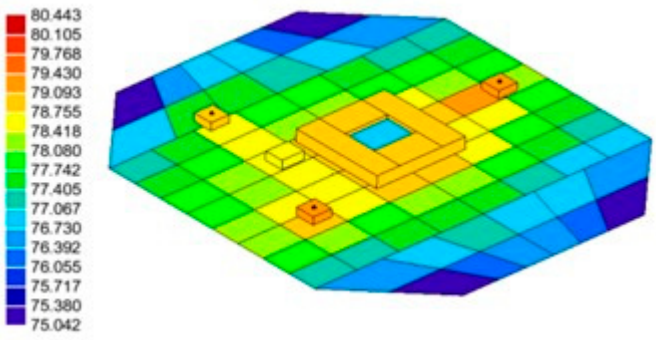



**Figure 11.** STR Hot Operational Case at a Sun exclusion angle of 18.5°.

(ii) Hot Operational Case (with Solar irradiation directly falling on the image sensor)

The temperature map for the Hot Operational Case where the STR is directly exposed to the Sun is shown in Figure 12.

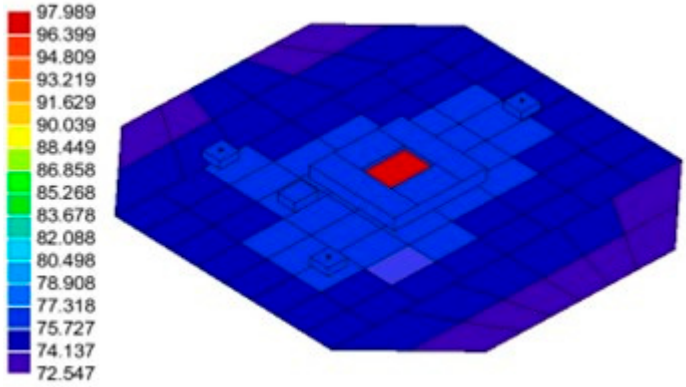



**Figure 12.** STR Hot Operational Case for direct Sun exposure.

In Figure 12, the temperature of the board ranges between 72.55 °C and 97.98 °C. The results indicate that the electronics exceeded their maximum temperature derated limits, potentially leading to component failure or even total PCB damage. Consequently, the OBCS must avoid direct Sun exposure, as it compromises operational integrity. The thermal design of the STR instrument has mitigation strategies to reduce the maximum temperatures due to extreme Solar exposure conditions.

(iii) STR Cold Non-Operational Case

For this case, the following characteristics/parameters are relevant:

(a) Nominal steady-state;
(b) Mechanical interface temperature: −10 °C;
(c) Ambient temperature: −270.15 °C;
(d) The EEEs are non-operational (STR fully Off).

The temperature map for the Cold Non-Operational Case where the STR is fully Off is shown in Figure 13.

In Figure 13, the temperature of the board ranges between −11.60 °C and −11.52 °C. The results confirm that all components remain well within their survival temperature limits, indicating no thermal risks in this state. The board is expected to resume operation without issues when powered back on.

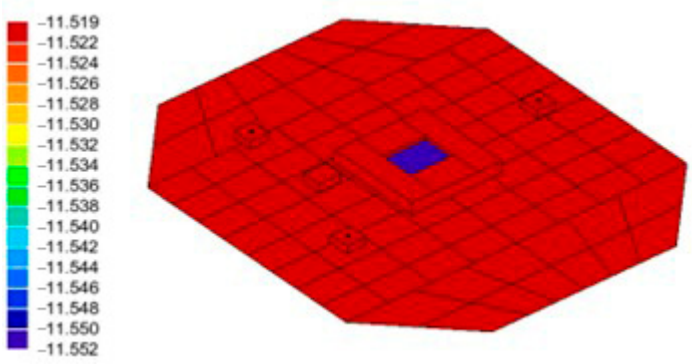



**Figure 13.** Fully Off STR Cold Non-Operational Case.

#### 6.2.3. Heat Dissipation Test

The ESATAN [17] simulations (Section 6.2.2) offered valuable insights into the thermal behavior of the star tracker in conditions simulating the space thermal environment. However, it was crucial to conduct real-world thermal measurements to understand the thermal behavior of the EEEs, mainly the processor and the image sensor. To accomplish this, the thermal camera model TC001-PLUS [21] was employed to evaluate heat distribution and component temperatures across various operational modes. The tests were conducted at a Synopsis Planet facility located in the Faculdade de Ciências, Universidade de Lisboa, Lisbon, Portugal. The STR's actual temperature map and heat dissipation video are shown in Figure 14 and in [22], respectively.

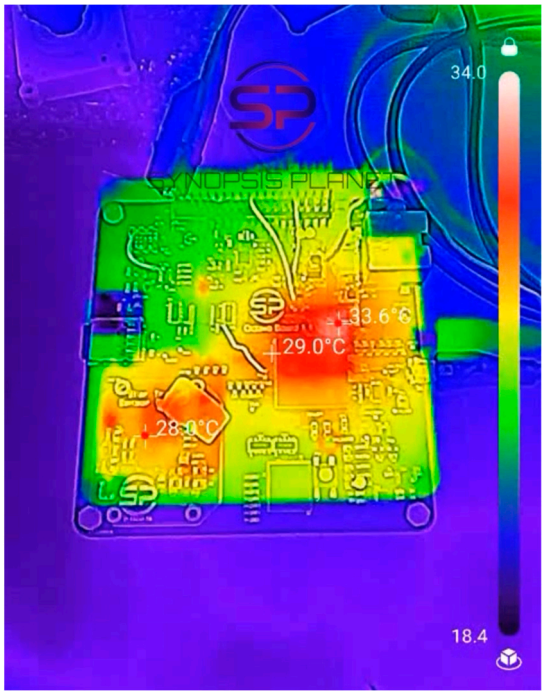



**Figure 14.** Casing temperature of the processor (center-right) and image sensor (bottom-left).

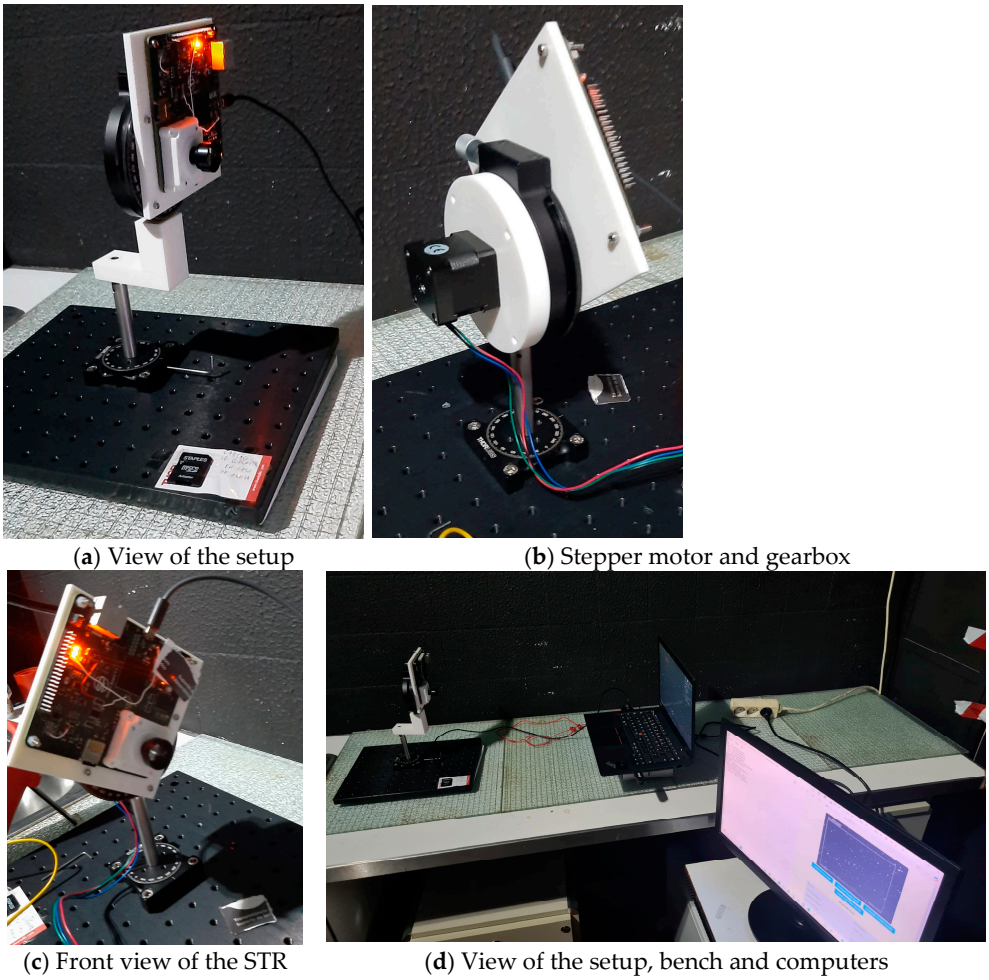
Figure 14 shows the CPU (processor) on the processor board as one of the main heat sources, reaching approximately 33.6 °C on the casing while executing the ASTRIDE [18]. Furthermore, when the sensor board was set to operate in video mode, the image sensor initially heated to around 28.0 °C, with heat gradually dissipating through the sensor PCB.

A thermal imaging video that illustrates how the components heat up and cool down across different operational modes can be viewed at following the link in [22].

These tests were performed in ambient conditions, i.e., at room temperature and with air in free convection. The tests mainly helped to validate the behavior of the crucial components of the STR. As seen in the thermal simulations, the processor heated up significantly during operation, and although the environmental conditions were different, the processor also heated up considerably in the tests.

### *6.3. Attitude Determination Setup Testing*

The attitude determination test is to validate the functionality of the attitude determination algorithms. To conduct the test inside the dark room, an experimental setup was developed with a stepper motor and gearbox that emulated the satellite's attitude. The test was conducted at Synopsis Planet, Faculdade de Ciências, Universidade de Lisboa, Lisbon, Portugal. The experimental test setup is shown in Figure 15.



(**a**) View of the setup (**b**) Stepper motor and gearbox

(**c**) Front view of the STR (**d**) View of the setup, bench and computers

**Figure 15.** Different views of the experimental test setup inside the dark room.

Figure 15a shows the view of the setup composed of the optical bench, the optical post with micrometric regulations and the STR connected to a stepper motor and a gearbox; Figure 15b shows the back view of the STR connected to the stepper motor and the gearbox; Figure 15c shows the front view of the STR and Figure 15d shows the view of the setup composed of the optical bench, the optical post, the STR, the laptop to run the Tetra3 algorithm [16] and the screen.

To conduct the test, the sensor and optical system parameters were set as follows:

(a) Resolution: 1280 × 960 px;
(b) Sensor size: 4.8 mm × 3.6 mm;

(c) Focal length: 16 mm;
(d) Aperture: f/13.33;
(e) FoV with lens: ≈17°;
(f) Digital gain: 1;
(g) Integration multiplication factor: 1000 (corresponding to an exposure time of 22.2 ms);
(h) Monitor screen brightness was set to the lowest possible level to avoid interference from ambient light;
(i) A reference star image from the sky was generated using Stellarium Web [15], with the sensor and lens parameters configured to match the test conditions.

Test Procedure

The test procedure validates the functionality of the attitude determination algorithms. The STR system was tested by capturing an image, running the Tetra3 algorithm [16] and verifying whether the computed Right Ascension (RA) and Declination (Dec) values corresponded to those in the selected reference image.

In the dark room with the test setup, the STR is turned on, operating in Tetra3 mode for star identification. During the test, the sky reference image from Stellarium Web is displayed on the screen. The captured image from the STR sensor is then compared to this reference. It is crucial for the captured image to closely align with the red guideline margins in Stellarium to ensure the accurate position matching shown in Figure 16.

In Figure 16 the Tetra3 algorithm is executed on the captured image, yielding results that match the expected RA value, Dec value, roll value and camera FoV values from Stellarium Web [15] and Tetra3, as shown in Figure 17 and in Table 2.

**Table 2.** Comparison between Stellarium and Tetra3 for the RA and Dec parameters.

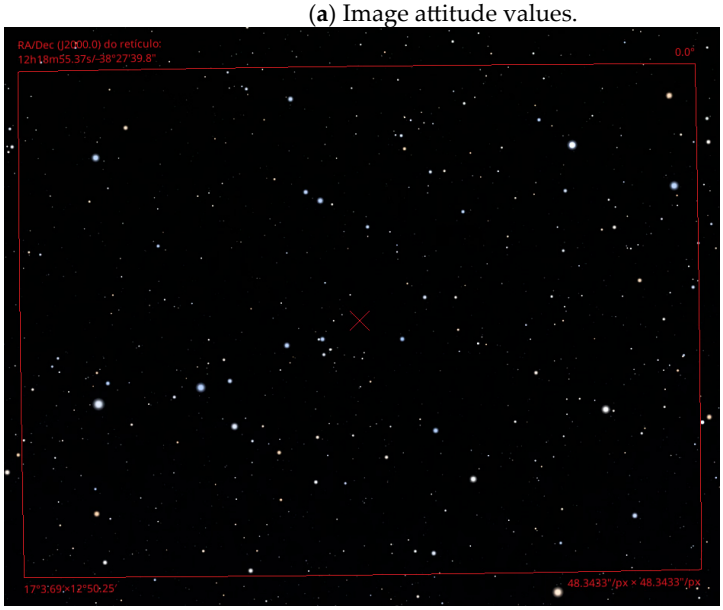
| Variables | Stellarium (deg) | Tetra3 (deg) | Difference (%) |
|---|---|---|---|
| RA | 184.73 (12 h 18 m 55.37 s) | 182.71 | 1.09 |
| Dec | −38.27 | −38.00 | 0.07 |

In Figure 17 the important values are the highlighted ones.

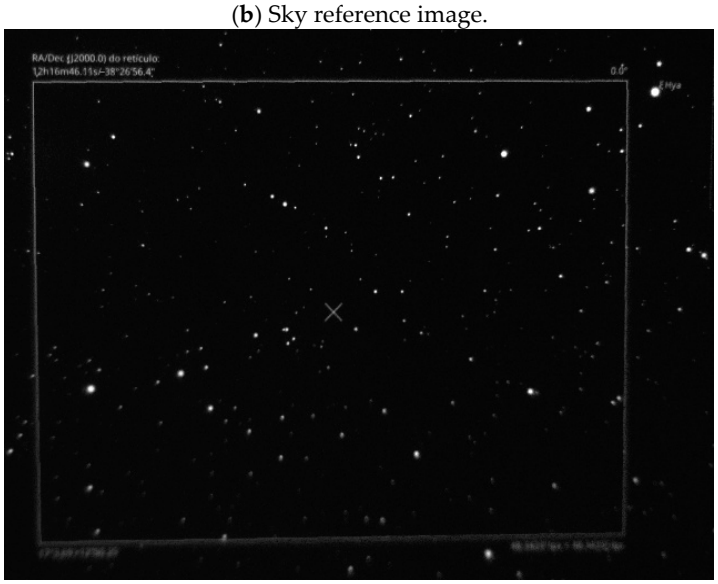
Figures 16 and 17 and Table 2 show that the RA value is 182.71°, the Dec value is -38.00°, the Roll value is 359.01° and the FoV value is 18.17°. The test successfully demonstrates that the star tracker camera is fully functional, and the image processing pipeline between the sensor and processor operates correctly. The accurate determination of RA and Dec confirms that the Tetra3 algorithm is properly integrated and capable of reliable star identification, validating the overall performance of the attitude determination system. Additionally, the FoV observed in the results closely matches the expected value with the lens on the sensor, further confirming the system's alignment with design specifications.

In Table 2, there is a slight discrepancy between the values provided by Stellarium and Tetra3. This occurs because Stellarium gives the exact coordinates of the center of the frame (marked by the red crosshair in Figure 16a,b), whereas the center of the image captured by the star tracker does not perfectly align with this point. Additionally, the star catalog used by Tetra3 may differ slightly from Stellarium's database, which can introduce minor variations in the attitude estimation. Despite these differences, the results are consistent enough to confirm the correct functioning of the attitude detection system.


(**a**) Image attitude values.




(**b**) Sky reference image.




(**c**) Image capture of the sky for the Tetra3 test.

**Figure 16.** Reference images from Stellarium and those captured for the Tetra3 test.

```
RA: 182.71465614994327
Dec: -38.0079873807833
Roll: 359.0187288320969
FOV: 18.1738935433902
```

**Figure 17.** Tetra3 results with expected RA, Dec, Roll and FoV values.

## 7. Conclusions

This paper has presented the successful design, development and validation of a miniature instrument for small satellites used as a dual-purpose device capable of performing both star tracking and space debris detection. Building upon prior conceptual- and breadboard-level implementations, the new miniature instrument marks a significant advancement by realizing a fully functional system composed of Commercial Off-the-Shelf components with proven space heritage. The adoption of a New Space development approach facilitated a cost-effective and modular design, promoting accessibility and rapid deployment in future space missions.

The experimental results validate the operational viability of the miniature instrument under realistic conditions, confirming its suitability for both attitude determination and orbital situational awareness. Furthermore, the modular architecture ensures scalability and adaptability to diverse mission profiles. Future work will focus on extending the detection capabilities, enhancing onboard processing and conducting in-orbit validation to further assess performance in the intended space environment.

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**Conflicts of Interest:** The authors declare no conflicts of interest.

## Abbreviations

The following abbreviations are used in this manuscript:

| | |
|---|---|
| BGA | Ball grid array package |
| CAN-bus | Controller area network bus |
| CCD | Charge-Coupled Device |
| CMOS | Complementary metal–oxide–semiconductor |
| COTS | Commercial Off-the-Shelf |
| CPU | Central processing unit |
| Dec | Declination |
| EDAC | Error detection and correction |
| EEEs | All electronic components |

| | |
|---|---|
| eMMC | Embedded MultiMediaCard |
| FoV | Field-of-View |
| FPGA | Field-programmable gate array |
| fps | Frames per second |
| I2C | Inter-integrated circuit |
| LCC | Lead-less chip carrier |
| LEO | Low Earth Orbit |
| OBCS | Onboard computer system |
| PCB | Printed circuit board |
| PLL | Phase-Locked Loop |
| PMU | Power Management Unit |
| PRU | Programmable Real-Time Unit |
| RA | Right Ascension |
| SD card | Secure Digital card |
| SNR | Signal-to-noise ratio |
| STR | Star tracker |
| UART | Universal asynchronous receiver–transmitter |

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