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Fault Tolerant DC–DC Converters at Homes and Offices

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Thesis submitted for the fulfilment of the requirements for the degree of
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Declaração de Integridade

Eu, Fernando José Figueiredo Bento, que abaixo assino, estudante com o número de inscrição D1976, do curso Engenharia Eletrotécnica e de Computadores da Faculdade de Engenharia, declaro ter desenvolvido o presente trabalho e elaborado o presente texto em total consonância com o **Código de Integridades da Universidade da Beira Interior**.

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Dedication

This thesis is dedicated to the beloved memory of my grandmother Ilda, grandfather Manuel Figueiredo, and Godmother Maria do Carmo, unique persons that served as references of resilience, devotion, and humbleness.

Also, I would like to extend my dedication to the memory of André da Silva Barcelos, a close friend and research colleague that passed away recently.

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Accomplishing this target was something that I would never imagine at all until very recently. Such achievement was just possible due to the contribution and effort of many people, to whom I would like to express my deepest appreciation. First of all, I want to thank to all my family, especially my parents, sisters, and brothers, for the patience and constant support given during this long journey.

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Abstract

The emergence of direct current (DC) microgrids within the context of residential buildings and offices brings in a whole new paradigm in energy distribution. As a result, a set of technical challenges arise, concerning the adoption of efficient, cost-effective, and reliable DC-compatible power conditioning solutions, suitable to interface DC microgrids and energy consuming elements.

This thesis encompasses the development of DC–DC power conversion solutions, featuring improved availability and efficiency, suitable to meet the requirements of a comprehensive set of end-uses commonly found in homes and offices.

Based on the energy consumption profiles and requirements of the typical elements found at homes and offices, three distinctive groups are established: light-emitting diode (LED) lighting, electric vehicle (EV) charging, and general appliances. For each group, a careful evaluation of the criteria to fulfil is performed, based on which at least one DC–DC power converter is selected and investigated. Totally, a set of five DC–DC converter topologies are addressed in this work, being specific aspects related to fault diagnosis and/or fault tolerance analysed with particular detail in two of them.

Firstly, mathematical models are described for LED devices and EV batteries, for the development of a theoretical analysis of the systems' operation through computational simulations.

Based on a compilation of requirements to account for in each end-use (LED lighting, EV charging, and general appliances), brief design considerations are drawn for each converter topology, regarding their architecture and control strategy.

Aiming a detailed understanding of the two DC–DC power conversion systems subjected to thorough evaluation in this work – interleaved boost converter and fault-tolerant single-inductor multiple-output (SIMO) converter – under both normal and abnormal conditions, the operation of the systems is evaluated in the presence of open-circuit (OC) faults. Parameters of interest are monitored and evaluated to understand how the failures impact the operation of the entire system. At this stage, valuable information is obtained for the development of fault diagnosis strategies.

Taking profit of the data collected in the analysis, a novel fault diagnostic strategy is presented, targeting interleaved DC–DC boost converters for general appliances. Ease of implementation, fast diagnostic and robustness against false alarms distinguish the proposed approach over the state-of-the-art. Its effectiveness is confirmed through a set of operation scenarios, implemented in both simulation environment and experimental context.

Finally, an extensive set of reconfiguration strategies is presented and evaluated, aiming to grant fault tolerance capability to the multiple DC–DC converter topologies under analysis. A hybrid reconfiguration approach is developed for the interleaved boost converter. It is demonstrated that the combination of reconfiguration strategies promotes remarkable improvements on the post-fault operation of the converter. In addition, an alternative SIMO converter architecture, featuring inherent tolerance against OC faults, is presented and described. To exploit the OC fault tolerance capability of the fault-tolerant SIMO converter, a converter topology targeted at residential LED lighting systems, two alternative reconfiguration strategies are presented and evaluated in detail. Results obtained from computational simulations and experimental tests confirm the effectiveness of the approaches. To further improve the fault-tolerant SIMO converter with regards to its robustness against sensor faults, while simplifying its hardware architecture, a sensorless current control strategy is presented. The proposed control strategy is evaluated resorting to computational simulations.

Keywords

Homes; Offices; DC microgrids; DC–DC converters; Fault diagnosis; Fault tolerance; LED lighting; EV charging; General appliances.

Resumo alargado

O surgimento de micro-redes em corrente contínua (CC) em edifícios residenciais e de escritórios estabelece um novo paradigma no domínio da distribuição de energia. Como consequência disso, surge uma panóplia de desafios técnicos ligados à adopção de soluções de conversão de energia, compatíveis com CC, que demonstrem ser eficientes, rentáveis e fiáveis, capazes de estabelecer a interface entre micro-redes em CC e as cargas alimentadas por esse sistema de energia.

Até aos dias de hoje, os conversores CC–CC têm vindo a ser maioritariamente utilizados em aplicações de nicho, que geralmente envolvem níveis de potência reduzidos. Porém, as perspectivas futuras apontam para a adopção, em larga escala, destas tecnologias de conversão de energia, também em equipamentos eléctricos residenciais e de escritórios. Tal como qualquer outra tecnologia de conversão electrónica de potência, os conversores CC–CC podem ver o seu funcionamento afectado por falhas que degradam o seu bom funcionamento, sendo que essas falhas acabam por afectar não apenas os conversores em si, mas também as cargas que alimentam, limitando assim o tempo de vida útil do conjunto conversor + carga. Desta forma, é fulcral localizar a origem da falha, para que possam ser adoptadas acções correctivas, capazes de limitar as consequências nefastas associadas à falha.

Para responder a este desafio, esta tese contempla o desenvolvimento de soluções de conversão de energia CC–CC altamente eficientes e fiáveis, capazes de responder a requisitos impostos por um conjunto alargado de equipamentos frequentemente encontrados em habitações e escritórios.

Com base nos perfis de consumo de energia eléctrica e nos requisitos impostos pelas cargas tipicamente utilizadas em habitações e escritórios, são estabelecidos três grupos distintos: iluminação através de díodos emissores de luz, carregamento de veículo eléctrico (VE) e aparelhos eléctricos em geral. Para cada grupo, é efectuada uma avaliação cuidadosa dos critérios a respeitar, sendo com base nesses critérios que será escolhida e investigada pelo menos uma topologia de conversor CC–CC. No total, são abordadas cinco topologias de conversores CC–CC distintas, sendo que os aspectos ligados ao diagnóstico de avarias e/ou tolerância a falhas são analisados com particular detalhe em duas dessas topologias.

Inicialmente, são estabelecidos modelos matemáticos descritivos do comportamento das principais cargas consideradas no estudo – díodos emissores de luz e baterias de VEs – visando a análise teórica do funcionamento dos sistemas em estudo, suportada por simulações computacionais.

Com base numa compilação de requisitos a ter em conta em cada aplicação – iluminação através de díodos emissores de luz, carregamento de veículo eléctrico (VE) e aparelhos eléctricos em geral – são estabelecidas considerações ligadas à escolha de cada topologia de conversor não isolado, no que respeita à sua arquitectura e estratégia de controlo.

Visando o conhecimento aprofundado das duas topologias de conversor CC–CC alvo de particular enfoque neste trabalho – conversor entrelaçado elevador e conversor de entrada única e múltiplas saídas, tolerante a falhas – quer em funcionamento normal, quer em funcionamento em modo de falha, é avaliado o funcionamento de ambas as topologias na presença de falhas de circuito aberto nos semicondutores activos. Para o efeito, são monitorizados e analisados parâmetros úteis à percepção da forma como os modos de falha avaliados neste trabalho impactam o funcionamento de todo o sistema. Nesta fase, é obtida informação fundamental ao desenvolvimento de estratégias de diagnóstico de avarias, particularmente indicadas para avarias de circuito aberto nos semicondutores activos dos conversores em estudo.

Com base na informação recolhida anteriormente, é apresentada uma nova estratégia de diagnóstico de avarias direccionada a conversores CC–CC elevadores entrelaçados utilizados em aparelhos eléctricos, em geral. Facilidade de implementação, rapidez e robustez contra falsos positivos são algumas das características que distinguem a estratégia proposta em relação ao estado da arte. A sua efectividade é confirmada com recurso a uma multiplicidade de cenários de funcionamento, implementados quer em ambiente de simulação, quer em contexto experimental.

Por fim, é apresentada e avaliada uma gama alargada de estratégias de reconfiguração, que visam assegurar a tolerância a falhas das diversas topologias de conversores CC–CC em estudo. É desenvolvida uma estratégia de reconfiguração híbrida, direccionada ao conversor entrelaçado elevador, que combina múltiplas medidas de reconfiguração mais simples num único procedimento. Demonstra-se que a combinação de múltiplas estratégias de reconfiguração introduz melhorias substanciais no funcionamento do conversor ao longo do período pós-falha, ao mesmo tempo que assegura a manutenção da qualidade da energia à entrada e saída do conversor reconfigurado. Noutra frente, é apresentada e descrita uma arquitectura alternativa do conversor de entrada única e múltiplas saídas, com tolerância a falhas de circuito aberto. Através da configuração proposta, é possível manter o fornecimento de energia eléctrica a todas as saídas do conversor. Para tirar máximo proveito da tolerância a falhas do conversor de entrada única e múltiplas saídas, uma topologia de conversor indicada para sistemas residenciais de iluminação baseados em díodos emissores de luz, são apresentadas e avaliadas duas estratégias de reconfiguração do conversor, exclusivamente baseadas na adaptação do

controlo aplicado ao conversor. Os resultados de simulação computacional e os resultados experimentais obtidos confirmam a efectividade das abordagens adoptadas, através da melhoria da qualidade da energia eléctrica fornecida às diversas saídas do conversor. São assim asseguradas condições essenciais ao funcionamento ininterrupto e estável dos sistemas de iluminação, já que a qualidade da energia eléctrica fornecida aos sistemas de iluminação tem impacto directo na qualidade da luz produzida. Por fim, e para aprimorar o conversor de entrada única e múltiplas saídas tolerante a falhas, no que respeita à sua robustez contra falhas em sensores, é apresentada uma estratégia de controlo de corrente que evita o recurso excessivo a sensores e, ao mesmo tempo, simplifica a estrutura de controlo do conversor. A estratégia apresentada é avaliada através de simulações computacionais. A abordagem apresentada assume vantagens em múltiplos domínios, sendo de destacar vantagens como a melhoria da fiabilidade de todo o sistema de iluminação (conversor + carga), os ganhos atingidos ao nível do rendimento, a redução do custo de implementação da solução, ou a simplificação da estrutura de controlo.

Palavras-chave

Habitações; Escritórios; Micro-redes CC; Conversores CC–CC; Diagnóstico de avarias; Tolerância a falhas; Iluminação através de díodos emissores de luz; Carregamento de veículos eléctricos; Aplicações domésticas.

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Nomenclature

AC	Alternating Current
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ESS	Energy Storage System
EV	Electric Vehicle
FB	Full Bridge
FFT	Fast Fourier Transform
G2V	Grid-to-Vehicle
HB	Half Bridge
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IPOS	Input-Parallel Output-Series
ISOP	Input-Series Output-Parallel
ISOSP	Input-Series Output-Series/Parallel
LED	Light Emitting Diode
LLC	Inductor-Inductor-Capacitor
MMC	Modular Multilevel Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
OC	Open-Circuit
PFC	Power Factor Correction
PI	Proportional-Integral
PSFB	Phase-Shifted Full-Bridge
PV	Photovoltaic
PWM	Pulse Width Modulation
SAB	Single Active Bridge
SC	Short-Circuit

SEPIC	Single-Ended Primary-Inductor Converter
SIMO	Single-Inductor Multiple-Output
SSR	Solid-State Relay
THD	Total Harmonic Distortion
TLA	Temporal Light Artifact
TRIAC	Triode for Alternating Current
V2G	Vehicle-to-Grid
VFD	Variable Frequency Drive
ZVS	Zero-Voltage Switching

Chapter 1

Introduction

Fighting climate change surge is a challenging goal that mankind seeks to solve by all means necessary. Energy transition ascertains itself as a promising mean for fighting climate change, by defining a pathway towards transformation of the global energy sector from fossil-based to zero-carbon. Energy transition embraces a multitude of measures and involves tangible actions, transversal to multiple sectors of activity – industry, transportation, or primary sector, to name a few. Among other measures, the adoption of more efficient and sustainable energy distribution systems stands out. Structural changes in the paradigm of energy distribution, as it is the transition to direct current (DC) microgrids deployed in the context of homes and offices, reveals extremely promising, not only to optimise the efficiency of energy distribution systems, but also to reduce the utilisation of some expensive and unreliable technical resources.

The roster of benefits associated to DC microgrids is continuously increasing, thanks to a favourable context and a series of technological evolutions, observed at homes and offices, in three distinctive and well-defined vectors – microgeneration, energy consumption, and storage.

Over time, the totally passive position of homes and offices within the electric energy market has shifted towards a very active position, due to the large-scale deployment of microgeneration systems [1]. Most of these systems, mainly consisting of solar photovoltaic (PV) panels and wind turbine systems, are DC-compatible or involve, at a certain stage, the conversion of alternating current (AC) to DC.

In turn, recent advancements in technology led to the increase of the electronic equipment used in private homes and offices. Most of this equipment is DC powered, meaning that AC–DC and/or DC–AC converters have to be applied as interface between the load and the currently established AC grid. Integrated in the DC bus of the AC–DC and DC–AC converters, it is sometimes possible to also find DC–DC converters, responsible for power factor correction or for providing galvanic isolation. Unfortunately, the efficiency of AC–DC and DC–AC converters is quite limited, as the conversion process is highly inefficient and takes several steps to complete [2]. Studies demonstrate that the energy consumption associated with DC-compatible or potentially DC-compatible loads accounted for roughly 50 % of the overall energy consumption in an average home from Europe-27, in

the year 2009 [3]. The evolution of indicators like the fast-growing adoption of electric vehicle (EV) charging, the penetration of general appliances with variable frequency drives (VFDs), or the significantly higher adoption of light emitting diode (LED) lighting, provide a solid clue about the strong contribution of DC-compatible loads to the overall energy consumption [4].

As expected, DC compatibility prevails within the group of technologies associated to the third vector – energy storage. Batteries and supercapacitors are two well-known energy storage technologies that operate in DC, that are expected to gain relevance in homes and offices.

A natural consequence of the broad adoption of DC-compatible technologies, extensive to all three vectors, is the large-scale promotion of inefficiencies on the power conversion processes. Fig. 1.1 represents an illustration of a residential building, supplied through a common AC energy distribution system. The schematic contains the most representative elements of an energy system. Microgeneration technologies are represented by the PV system and the small-scale wind turbine. As for the energy consumption elements, the schematic adopts different colours for the wiring. LED lighting systems are associated to the yellow wiring; general appliances with VFDs are associated to the brown wiring; other general appliances are associated to the blue wiring; and the EV charging is associated to the green wiring. In turn, energy storage is represented in the schematic by a battery. All the elements of the energy system establish the interface with the AC bus resorting to AC–DC and, in some cases, DC–AC energy conversion technologies. In Fig. 1.1, such energy conversion technologies are represented along with the corresponding power conversion losses. An evaluation to Fig. 1.1 reveals that up to 20 % of the energy can be lost in each energy conversion process.

The shift on the paradigm of energy generation, storage, and consumption is leveraging the interests on the adoption of DC technologies, on a district scale. Broad adoption of DC microgrids provides an effective mean to secure important energy savings in residential buildings and offices. Fig. 1.2 depicts the structure of a residential building whose energy distribution system is based on DC technology. If a comparison is established between the AC-based energy distribution system (Fig. 1.1) and the DC-based one (Fig. 1.2), it is noticed that the energy conversion losses are greatly curtailed, thanks to the significant simplification of the power conversion procedures, observed in DC microgrids. The potential of DC microgrids and DC–DC converters to minimise the power losses at the residential energy distribution level is also pointed out on a set of case studies that establish comparisons between typical AC energy systems and novel DC microgrids [5]–[7].

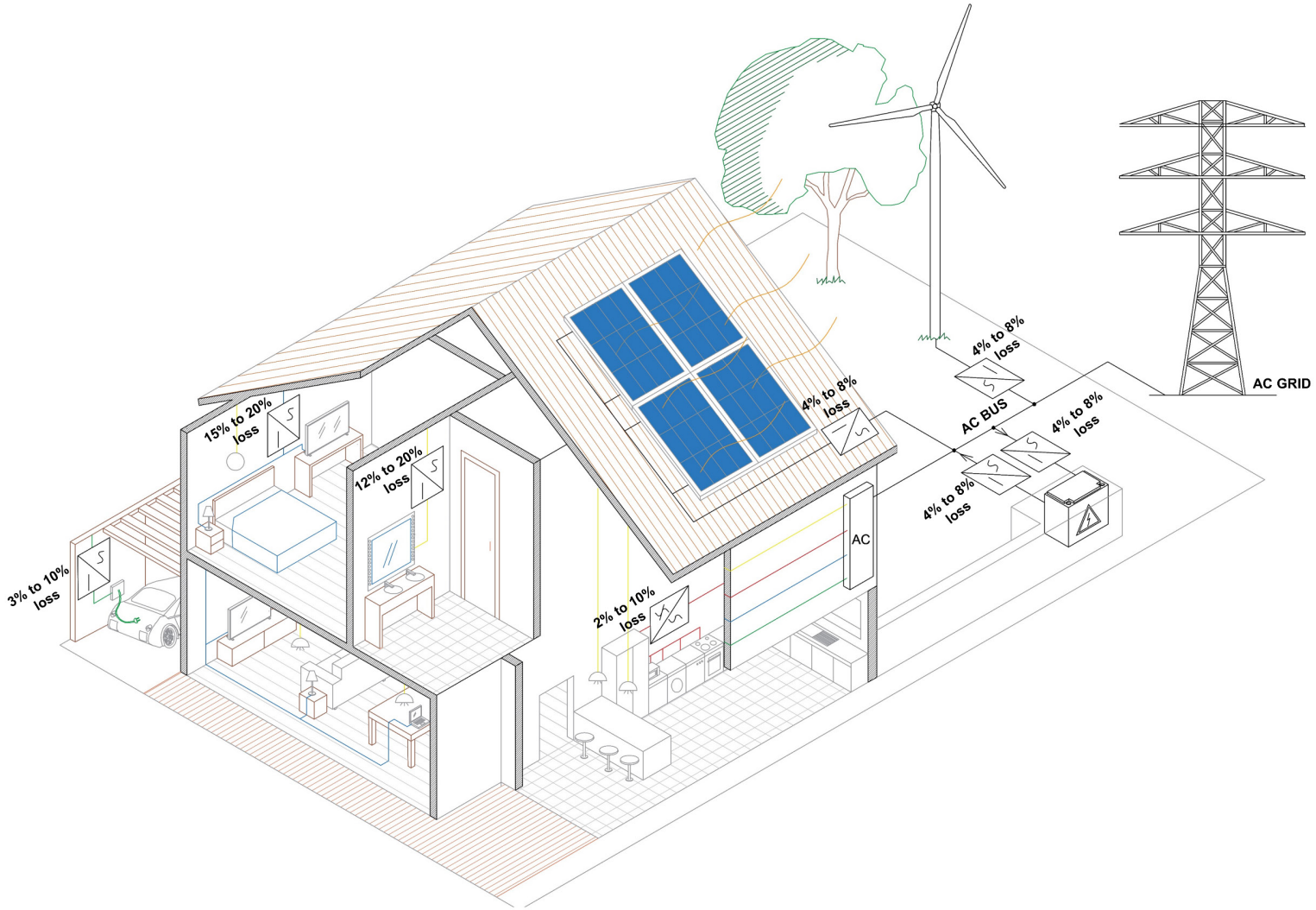


Fig. 1.1 Schematic representation of a residential building supplied by an AC energy distribution system, including typical energy conversion stages and related power conversion losses [4].

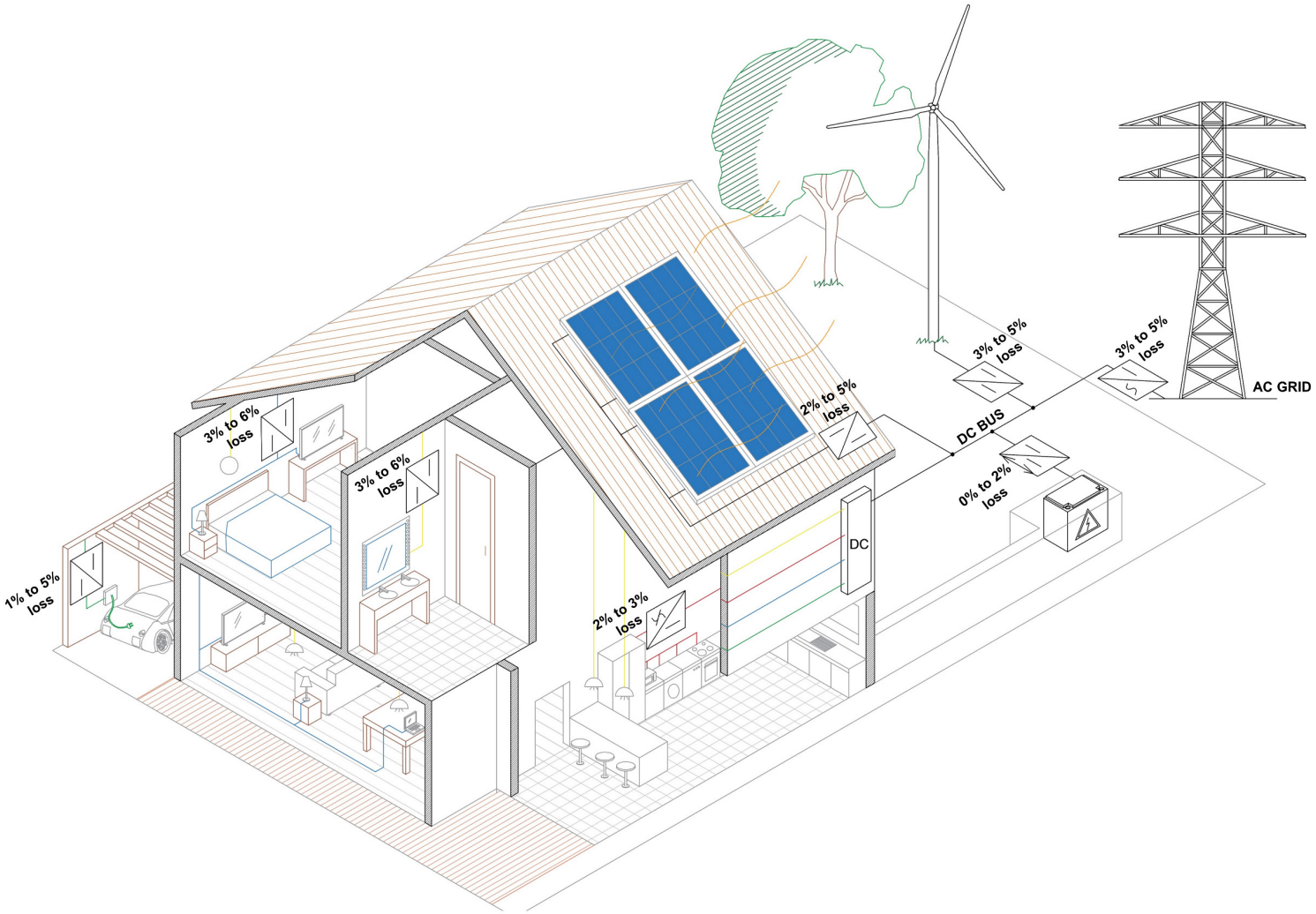


Fig. 1.2 Schematic representation of a residential building supplied by a DC energy distribution system, including typical energy conversion stages and related power conversion losses [4].

To accelerate the transition towards a framework of broad adoption of DC microgrids, while assuring a smooth transition, standardisation is one of the key aspects. With that goal in mind, the Institute of Electrical and Electronics Engineers (IEEE) European Public Policy Committee issued a set of recommendations targeted at European authorities [8], aiming a coordinated action from key stakeholders with potential involvement in the process of implementation of DC microgrids.

The numbers and metrics provided in case studies evaluating the implementation of district-scale DC microgrids are indeed extremely encouraging and compelling. Nevertheless, there are an important set of technological hurdles which remain in place. Many DC technologies are yet to be developed or are now giving their first steps. DC–DC power conversion and DC protection systems are two good examples of relatively recent technologies which require further developments to enable a smooth and large-scale transition to DC microgrids.

DC–DC converters are critical components of any DC microgrid. As shown in Fig. 1.2, DC–DC converters are mandatory to establish the interface between the DC bus and any of the elements of the DC microgrid, whether they belong to the vector 'microgeneration', to the vector 'energy consumption' or to the vector 'storage'. Given the context of implementation (residential buildings and offices), it is natural that the cost of implementation of any technology arises as a concern. Therefore, it is expected that low-cost DC–DC power converters, able to ensure high efficiency, high reliability, and low current ripple, will be frequently requested for such purposes.

Apart being sensitive elements, DC–DC converters are often exposed to stressful operation conditions, induced by electrical and/or thermal stress, making them very prone to fail. Power semiconductors, capacitors, and gate drivers are responsible for most of the failures in a power converter [9]. The development of fault diagnostic methods and fault tolerance strategies, targeted at the most susceptible components of power converters, improves the availability of power converters and increases the interest on their target applications – in this case, DC microgrids for homes and offices.

Open-circuit (OC) faults on the power semiconductors are among the most common and, at the same time, among the most critical failure modes of DC–DC converters. The scientific literature provides a reasonable set of fault diagnostic methods capable of dealing with such failure mode, albeit with important gaps. Most state-of-the-art fault diagnostic algorithms are restricted to specific DC–DC converters; some focus certain operation points; while others have a broad spectrum of action, but are too complicated for implementation in simple systems or have significant fault diagnostic times. More recently, the emergence of sophisticated digital signal processors (DSPs) triggered the development of fault diagnostic algorithms based on the converter model [10], [11]. The derivation of such

converter models may be particularly challenging in converters with a significant number of components. Moreover, the real-time emulation of the converter response implies a significant computational effort, which is not desirable at all in power conversion solutions for residential buildings.

Deployment of fault diagnostic methods should be closely followed by the implementation of fault tolerant strategies, so that continuous converter operation is secured, with acceptable quality levels. It is relevant to maintain the fault-tolerant converter hardware structure as simple as possible. Naturally, a fault-tolerant converter without any additional hardware represents the most interesting solution. The state-of-the-art on fault-tolerant DC–DC converters lacks simple solutions, featuring inherent fault tolerance. Besides, most of the solutions are not indicated for end-uses like LED lighting or EV charging.

To streamline the development of efficient and reliable district-scale DC microgrids, this thesis proposes a set of solutions that facilitate the implementation of fault diagnostic and fault tolerance capabilities on DC–DC converters intended for the multitude of end-uses commonly found in such DC microgrids.

Within the group of three vectors embraced by district-scale DC microgrids (microgeneration, energy consumption, and storage), this work focuses attentions on the energy storage and energy consumption elements and related DC–DC converters.

1.1. Outline and Contributions

The establishment of highly efficient and reliable DC microgrids in the context of homes and offices will allow large important savings and will promote the benefits of the green economy. It will also enable a massive cut in the global dependence on fossil fuels to produce energy and, consequently, a reduction of the growth in electricity costs.

This thesis contributes to the achievement of these very important goals, providing key contributions in the promotion of efficient and reliable DC microgrids in the context of homes and offices, considered to be a major step towards zero net energy buildings. Such goals are accomplished through the development of novel fault diagnosis and fault tolerant strategies, suitable to attain more efficient and reliable DC–DC converters.

Given the very early stage of development of technologies required for DC microgrids, the subject of work of this thesis encompasses the topics of performance analysis, fault diagnosis, and fault tolerance of DC–DC converters.

Since the design and architecture of DC microgrids is far from being fully consolidated, this thesis carries out an informed evaluation and selection of the preferable DC–DC converter topologies for each end-use. End-uses are grouped, according to their electrical characteristics and energy consumption profiles, into three distinctive categories:

general appliances, LED lighting, and EV charging. At least two distinctive converter topologies are selected for each category, based on a set of requirements considered more prominent and compelling within each category. Requirements like power converter ratings and number of converter outputs are considered.

The selected power conversion solutions are then evaluated and considered for the development of novel fault diagnosis and fault tolerant strategies, suitable to fulfil the particular requirements of low cost and low implementation effort, critical within the context of homes and offices. Even though the literature provides a reasonable set of strategies for the diagnostic of OC faults, such tools are unable to combine low cost, simplicity, and effectiveness in a single solution, while obviating dependence from the converter parameters and/or operation conditions. Accordingly, a novel semiconductor fault diagnosis strategy, capable of fulfilling all the aforementioned requirements, is developed for interleaved converters.

Moreover, an extensive roster of unique power conversion solutions featuring fault tolerance are introduced in this work. Thanks to their simplicity, they are particularly well suited for DC microgrids deployed in the context of homes and offices. The roster of novel solutions includes an improved reconfiguration strategy targeted at interleaved converters, a fault-tolerant single-inductor multiple-output (SIMO) converter architecture indicated for LED lighting applications, two reconfiguration strategies suitable to ameliorate the post-fault operation of the fault-tolerant SIMO converter, and a sensorless current control strategy indicated to improve the resilience of the fault-tolerant SIMO converter against eventual sensor faults.

In addition, this thesis contributes to the enlightened selection of DC–DC power conversion technologies for DC microgrids. The comparative performance evaluation developed in this work, not yet available in the scientific literature, provides the pros and cons of candidate DC–DC converters for each end-use.

1.2. Organisation of the Thesis

This work is structured into eight chapters. Chapter 1 introduces the work developed in the thesis. It provides the contextualisation of the work, the motivation for the development of technologies for more efficient and reliable DC microgrids, and the identification of the gaps on the research related to DC microgrids, paying particular attention to the domains of fault diagnosis and fault tolerance of DC–DC converters.

Chapter 2 describes the processes of modelling and analysis of homes and offices appliances. Based on the evaluation to the scientific literature, analytical models of the most representative end-uses are derived and evaluated. Models of LEDs and batteries are presented.

Chapter 3 lists the DC–DC power conversion technologies capable of better fulfilling the requirements of end-use. The set of requirements associated to each end-use supports the selection of the best DC–DC converters. The presentation of the selected DC–DC converters is complemented with description of the control strategies considered for each converter.

In chapter 4, the operation principles of the DC–DC converters studied in this work are presented. Firstly, both healthy and faulty operation conditions are evaluated resorting to analytical calculations. Then, simulation and experimental data confirm the previously obtained analytical results.

Chapter 5 is fully dedicated to the topic of fault diagnosis on DC–DC converters. The chapter begins with the presentation of a detailed description and critical evaluation of the state-of-the-art on semiconductor fault diagnosis strategies aimed at DC–DC converters. Then, the contributions made in this work are presented, starting with the description of the theoretical principles. The effectiveness of the fault diagnosis strategy is confirmed through a comprehensive set of converter operation scenarios, replicated in simulation and in experimental tests.

Contributions made in the domain of fault tolerance are presented in chapter 6. The chapter starts with the detailed description and evaluation of the state-of-the-art. Then, a hybrid reconfiguration strategy is developed for interleaved DC–DC converters. Aiming LED lighting applications, a comprehensive set of solutions are introduced. A novel fault-tolerant converter architecture is introduced and described. Following, two novel reconfiguration strategies are presented. These strategies aim to improve the operation of the fault-tolerant converter. Finally, a sensorless current control approach is developed. All aforementioned solutions are subjected to validation, under a variety of operation scenarios established in simulation and experimental environment.

Chapter 7 provides a comparative performance evaluation between the DC–DC converter topologies considered for LED lighting and EV charging applications. The comparison is made based on the following parameters: fault tolerance, cost of implementation, number of components, components stress, and efficiency.

The thesis finishes with the presentation of the main conclusions, in chapter 8. Proposals for future research directions complement this chapter.

Chapter 2

Modelling and analysis of homes and offices appliances

The use of DC energy and related technologies in the context of homes and offices faces its first stages of development. A plethora of research initiatives are now underway to develop all necessary technologies and seek for improvements in efficiency, reliability, and cost effectiveness. Therefore, there are still many developments to carry out towards the full understanding of DC microgrids and how the interactions between the grid, the loads, and the energy storage elements take place. In this regard, power conditioning assumes pivotal relevance, as the key element that establishes the interface between the DC microgrid and the appliances or the energy storage elements. The proper selection of the DC–DC converter topologies to carry out such interface therefore influences how the interface among the DC microgrid and the multiple energy consumption elements takes place. While selecting and designing the best solutions for power conditioning, it is desirable to be able to predict the behaviour of the appliances, namely through analytical models of those appliances.

This chapter provides a description of the analytical models developed in this work, targeted at homes and offices appliances. Being homes and offices characterised by hosting a multitude of equipment, mostly intended for energy consumption and energy storage, focus is put into the modelling of the elements considered more representative. Batteries are modelled and considered as the equipment integrated in energy storage systems; LED lights are modelled and considered as energy consuming systems; general appliances are herein represented, for simplicity, as resistive loads. Most general appliances integrate or consist of heating elements. Hence, modelling such loads as resistive elements provides a very good and straightforward mean, while allowing to properly evaluate the fault diagnostic and fault tolerant strategies proposed in this work.

2.1. LED strings

The LED lighting systems studied in this work consist of V-TAC LED strings. Table 2.1 lists the technical parameters of the LED string, provided by the manufacturer.

TABLE 2.1 LED STRING PARAMETERS

Parameter	Nomenclature	Value
No. of LEDs per string (connected in series)	m	15
Nominal voltage	$V_{n_{nom}}$	48 V
Nominal current	$I_{n_{nom}}$	0.22 A
Nominal power	$P_{n_{nom}}$	11 W

As stated in Table 2.1, the manufacturer provides very few information that allows to determine the analytical model of the LED string. Auxiliary data, extracted from experimental tests to the devices to study, are therefore required.

The electrical model of LED devices is characterised by the *V-I* curve, which provides the relation between the LED forward voltage and the LED forward current. It takes the form of an exponential function. Despite the fact that the response of LEDs is temperature-dependent [12], it is often sufficiently accurate to study the performance of LEDs at environmental temperatures (T = 25 °C), as long as the minimal temperature shift of the LED is ensured through proper cooling techniques. On that basis, the model implemented in this study neglects the temperature effect on the electrical performance of the LED.

In the domain of electrical engineering, modelling of elements characterised by an exponential function assumes challenging contours. For that reason, it is common to find in the literature studies where LEDs are modelled through a linear model [13]. For accuracy, the linear model relies on at least two distinctive sections. The first section is comprised in the interval [0 V_E] V, where V_E denotes the LED threshold voltage, i.e., the minimum voltage required to forward-bias the device and promote the beginning of conduction. When operated in this section, the LED device does not conduct current and, therefore, does not emit light. The second section is comprised in the interval [V_E V_{max}] V, where V_{max} denotes the maximum forward voltage supported by the device. This section represents the active region of the LED.

To improve the accuracy of the analytical model, approaching it to the exponential model, it is possible to opt by a piecewise linear model, composed of multiple linear sections [13].

The extrapolation of the linear model of the LED into an equivalent circuit takes place in a much straightforward and simple way. The model of each LED string consists of multiple individual LED devices, connected in series. In turn, each LED device is modelled as a series association of one ideal diode, one resistor, and one DC voltage source. Fig. 2.1 depicts the simplified equivalent model of the LED commonly adopted in the literature, which was also adopted in this study.

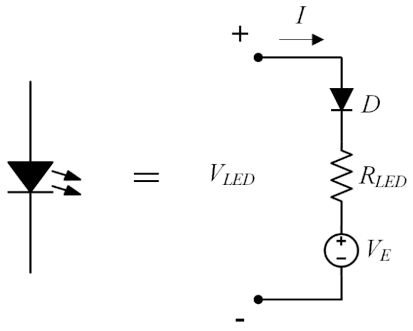


Fig. 2.1 Equivalent circuit of each LED device, based on the linear model approximation.

The manufacturer provides little information that allows to fully implement the analytical model of the LED string. To overcome such hurdle, simple experimental tests were conducted to determine the *V-I* curve representing the response of the LED string. Those tests, conducted at environment temperature, consist of connecting the LED string to a DC supply with controlled voltage. Multiple voltage levels are evaluated, in order to obtain multiple *V-I* pairs characteristic of the string. Fig. 2.2 depicts the data points obtained in the experimental tests and the resulting analytical model, to be considered for simulation purposes.

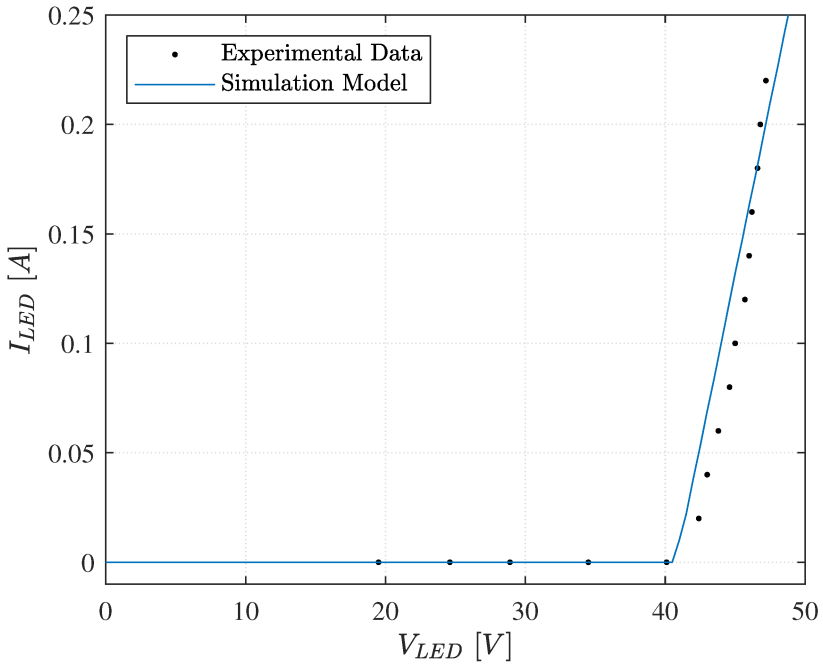


Fig. 2.2 *V-I* curve of the LED string; comparison between experimental data and the simulation model.

As observed in Fig. 2.2, there is a minor deviation between the analytical model and the experimental data, which was indeed expected. Still, such mismatch does not interfere with the quality of the results obtained through simulation. As LED strings are usually operated with current controllers rather than voltage controllers, the expected effect of the

slight mismatch between the two models is the observation of a minor error on the forward voltage of the LED.

Over the active region of the LED string, the analytical model is described by the following mathematical condition:

$$I_{LED} = 3.111 \times 10^{-2} V_{LED} - 1.268 \tag{2.1}$$

The analytical model described in (2.1) is effectively reproduced through the equivalent circuit represented in Fig. 2.1, considering the parameters of Table 2.2.

TABLE 2.2 PARAMETERS OF THE LED EQUIVALENT CIRCUIT

Parameter	Nomenclature	Value
Threshold voltage	V_E	40 V
On-state resistance	R_{LED}	32 Ω

Now, considering the same experimental data, it is possible to extract the exponential function that best describes the LED string being adopted. Fig. 2.3 depicts the experimental data and the resulting fit function, whose expression is provided in (2.2).

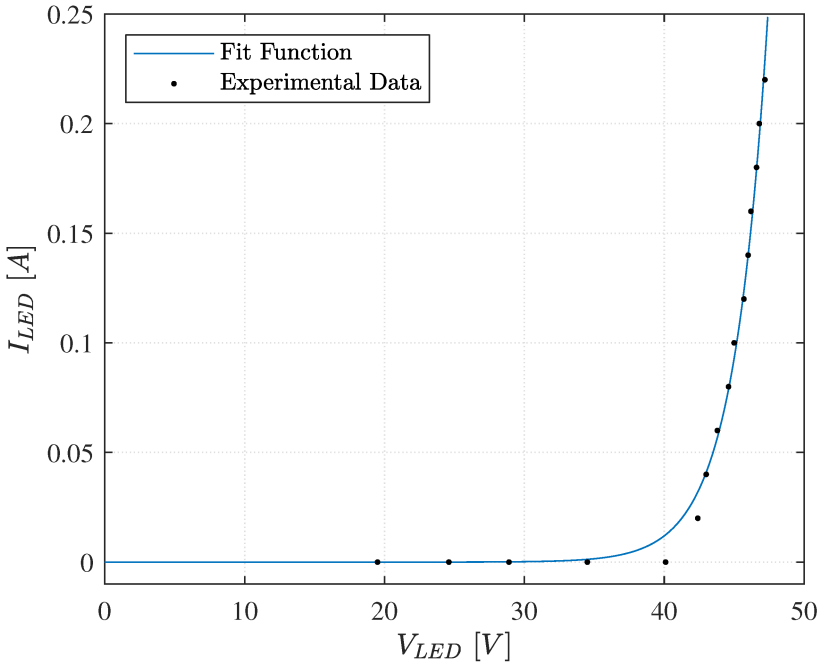


Fig. 2.3 Fit function obtained from the experimental data.

Resorting to MATLAB Curve Fitting toolbox to fit the experimental data into an exponential model, the following function is obtained:

$$I_{LED} = 8.981 \times 10^{-10} e^{0.4101 V_{LED}} \tag{2.2}$$

2.2. EV batteries

Modelling the batteries integrated in EVs reveals quite straightforward, given the multitude of tools and information available in the literature related to this subject. In fact, simulation software like *Simulink™* includes toolboxes that make the simulation of Li-ion batteries quite simple. To avoid redundancy, the analytical model of the battery is not described in detail in this thesis. For detailed information regarding the adopted Li-ion battery model, refer to [14].

The primary objective of this study is to employ batteries on energy storage systems, evaluating their behaviour and impact on the DC–DC converters responsible for managing the charging procedures over a short-term range. Therefore, considering long-term degradation phenomena of batteries present minor relevance. On that basis, the model does not account for temperature neither ageing effects, for simplicity.

Regarding the technical specifications, EV batteries are modelled according to the technical specifications of a battery pack integrated on a *Tesla Model S*. It has a capacity of 85 kWh (283 Ah), at a rated voltage of 300 V [15].

Chapter 3

Power conversion technologies for DC-supplied homes and offices

Nowadays, homes and offices are filled with a multitude of appliances, with distinctive end-uses and energy consumption patterns. Yet, homes and offices also host, more than ever, a series of elements with energy storage capabilities, ranging from electronics with small batteries to general energy storage systems comprised of batteries and/or related energy storage technologies. In a scenario of adoption of DC microgrids at residential buildings and offices, all the energy consumption and energy storage elements shall be powered by DC electricity, being the interface between the DC microgrid and those elements provided by highly efficient DC–DC converters. To answer to the requirements of the multitude of applications, it is critical to ensure the adoption of a broad selection of power conversion solutions, capable of meeting the specific requirements of each application, while promoting high efficiency in the power conversion processes. Indeed, the latter is particularly critical, as high efficiency is one of the flagships of DC microgrids. Even though DC microgrids are highly efficient by nature, thanks to their simplified architecture, DC–DC converters reveal a critical role in strengthening the performance of DC microgrids in terms of efficiency and availability. Hence, it is pivotal to take enlightened options regarding the selection of the DC–DC converter topologies that best fulfil the requirements of each end-use.

Following sections provide a brief description of the requirements that should be met for each application, followed by the presentation of the process of selection of the power conversion technologies suitable to handle the specific requirements of each end-use. Based on their characteristics and nature, the end-uses addressed in this work are grouped into three categories: general appliances, LED lighting, and EV charging.

3.1. General appliances

Apart LED lighting and EV charging, residential buildings and offices comprise a broad range of applications integrated into the energy systems: consumer electronics, televisions, washing machines, refrigerators, air conditioning systems, and so on. Finding

the best power conversion solutions, suitable to concurrently answer the stringent requirements imposed by most appliances, is a challenging task.

Very few references are found on the literature providing a detailed description of the development and application of DC–DC converters as the main power converter, establishing the interface between a DC supply and the appliance [16]–[19]. Indeed, an approach based on the retrofitting from AC to DC is commonly performed in those studies [18], [19]. In practice, this means that appliances whose original power supply was performed in AC are modified and adapted. Only part of the power supply circuitry is reconfigured, while the components useful for DC supply remain unchanged [18]. Usually, the challenge of selection and design of the best power converters is not considered in those studies, or the design of the power circuitry remains fairly sub-optimised.

In the few studies where the power supply is designed from the scratch, considering a direct connection to DC, the interleaved converter and the resonant converter are considered for general appliances [16].

Given the wide range of appliances framed in the category of general appliances, it is difficult to define a unique set of requirements. Nevertheless, it is possible to name the ones that are more relevant and cross-sectional. Regardless of the nature of the appliance to supply (VFD, heating elements, etc.), it is important to consider power converters capable of providing high efficiency, low cost, fault tolerance, and high-quality power.

With regards to fault tolerance, preference falls upon converters whose architecture is inherently tolerant against the most common and critical failure modes. The interleaved converter is, by excellence, the non-isolated converter capable of addressing this aspect more effectively.

Cost is also an important criterion to consider. Thanks to their simplicity, non-isolated DC–DC converter are usually more cost attractive. As one of the non-isolated DC–DC converters capable of limiting the most of the noise and perturbations at the converter output, the interleaved DC–DC converter reveals potential for supplying general appliances.

Given the set of requirements listed above, and considering the extended range of DC–DC converters with potential compatibility with such requirements, this work opts by the study of the non-isolated unidirectional interleaved boost converter. Interleaved DC–DC converters are extremely versatile power conversion solutions, featuring inherent tolerance against faults, as well as good conversion efficiency and reduced noise at the output.

Fig. 3.1 depicts the structure of a non-isolated unidirectional interleaved boost converter, suitable to ensure the integration of a broad range of household appliances into DC microgrids.

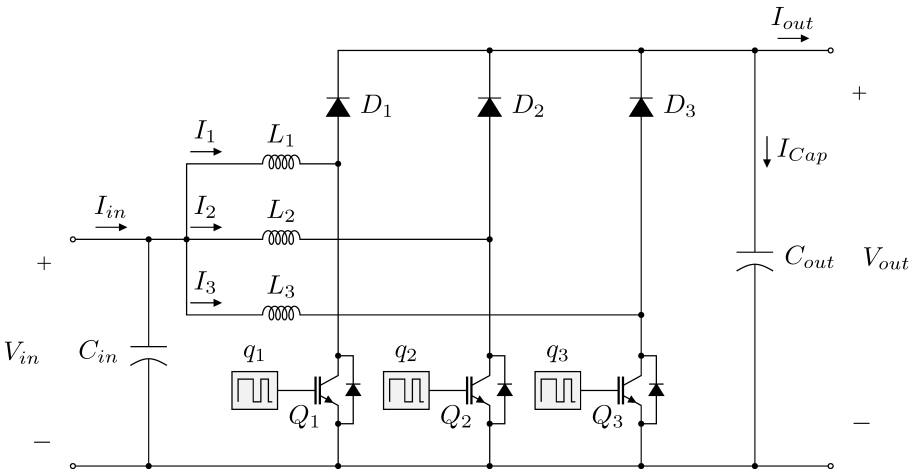


Fig. 3.1 Three-phase non-isolated unidirectional interleaved boost converter.

The proper selection of the number of converter phases plays an important role on aspects such as power conversion efficiency, cost or control complexity. Knowing in advance that low-power applications are dominant at homes and offices, and that simplicity of the requested power conversion solution is highly appreciated, it is reasonable to state that interleaved DC–DC converters with a large number of phases are not of particular interest. Keeping that in mind, it is reasonable to state that the interleaved boost converter with three phases provides a good balance between simplicity, and efficient power management, without compromising the high-quality power requirements demanded for general appliances.

3.1.1. Non-isolated unidirectional interleaved boost converter – control strategy

Depending on the conduction pattern of each phase inductor, this converter may operate in three distinctive modes: discontinuous conduction mode (DCM), boundary conduction mode (BCM) or continuous conduction mode (CCM). Each operation mode has its advantages and disadvantages. One of the major differences between DCM and CCM is the fact that conduction losses are dominant in DCM, whereas switching losses are the most important source of losses in a converter operating in CCM. Also, DCM typically implies fairly higher ripple on the converter currents – phase, input, and output currents. The latter fact usually promotes to the adoption of CCM as the conduction mode of preference. Unfortunately, converter operation in CCM compromises the voltage control strategy, causing serious current imbalance between converter phases, related to small differences between physical components, especially inductors, and mismatch in the duty cycles applied to each power switch.

Average current control can successfully solve most of the challenges associated to CCM. In this control strategy, two control loops are used: a voltage regulator and a current

regulator. The voltage control loop is the external loop and is responsible for adjusting the converter output voltage, resorting to a proportional-integral (PI) controller. This regulator uses a small bandwidth to avoid the negative effects of the input voltage ripple on the converter output voltage. The output of the voltage control loop defines the reference current I_{ref}, introduced as input of the second control loop. This loop, called the inner loop, is responsible for correcting the current error, defined as the difference between the reference current I_{ref} and the effective converter input current I_{in}. The current control loop has wide bandwidth, allowing it to track fast oscillations in the current reference signal. To effectively accomplish the average current control, both of the controlled variables (V_{out} and I_{in}) are sampled in precise instants, being the process of sampling synchronised resorting to the triangular carriers produced in the pulse width modulator. The single output of the current regulator provides the switching duty cycle d, to be introduced in the pulse width modulator.

Fig. 3.2 shows the architecture of the adopted average current control strategy.

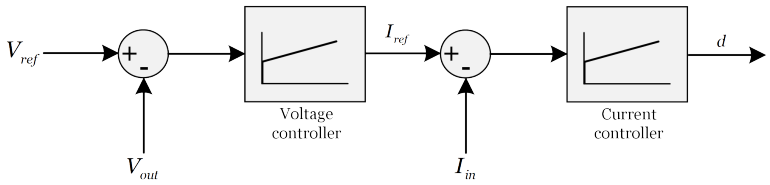


Fig. 3.2 Simplification of the control structure used to perform the average current control of the non-isolated unidirectional three-phase interleaved boost converter.

The parameters of the two PI controllers are compiled in Table 3.1 and Table 3.2.

TABLE 3.1 VOLTAGE CONTROLLER PARAMETERS

Parameter	Value
K_p	0.1
K_i	2

TABLE 3.2 CURRENT CONTROLLER PARAMETERS

Parameter	Value
K_p	0.1
K_i	20

Also note that, as the converter is composed of three phases, a phase-shift of $2\pi/3$ *rad* shall be applied between the three gating signals, so that the three phase currents produce an interleaved and balanced current pattern.

3.2. LED lighting

Lighting systems are among the most important elements of the electric energy systems found at homes and offices. Indeed, many research efforts have been developed in recent years to design more efficient and reliable lighting systems, giving particular emphasis on solid-state lighting technologies. Features like high efficiency, low power consumption, environmental friendliness, and long lifetime are just part of the criteria that weight on the selection of LED lighting technology for residential lighting systems [20], [21].

In the field of LED lighting, LEDs cannot be operated independently, requiring auxiliary circuitry dedicated to current control. Such auxiliary circuitry is commonly termed as 'drivers'.

LED lighting and related power electronics technologies are quite recent. Yet, the scientific literature already presents and describes in detail a plethora of LED driver architectures, with distinctive features and end-uses [22]. Switched-mode regulators are currently the preferred choice for supplying LEDs, due to the major benefits in terms of precise dimming control, excellent efficiency levels, and ease of control. Since the currently established electric energy systems are mostly based on AC, it is natural to witness that most switching mode LED driver architectures proposed in the literature are based on multi-stage AC–DC converters. The proposed AC–DC LED driver solutions have distinctive merits. Some aim to improve the performance at wider ranges of input voltage [23], while others aim at eliminating the electrolytic capacitors from the driver, without compromising the converter efficiency neither the quality of the produced light [24]–[26].

Regarding LED drivers based on DC–DC converter topologies, required to establish the interface between DC microgrids and the LED lighting systems, the flyback converter stands out as the most commonly employed LED driver topology, due to its simplicity and galvanic isolation feature [27]. Still, LED drivers inspired in generic topologies, like buck, boost, single-ended primary-inductor converter (SEPIC), and half-bridge (HB) converters are also considered in many cases. Among other DC–DC conversion technologies, the state-of-the-art includes developments on SIMO LED drivers [28], resonant buck converters [29], inductor-inductor-capacitor (LLC) resonant converters [30], integrated buck–boost–buck-type single-switch multistring resonant converters [31], single switch multi-stage DC–DC converters [32], and interleaved flyback converters [33], to name a few. Most of the listed configurations are designed to supply multiple LED strings with a single driver.

Recent studies are shifting the attention towards more elaborated and interesting LED driver topologies. LED lighting solutions currently available in the market, targeted at residential lighting applications, typically rely on dedicated drivers to control a single LED string. Nonetheless, this approach presents serious drawbacks from both technical and economical points of view. By including a LED driver on each string, a significant number

of commonly overrated components is employed to drive each LED string [34]. Besides, this approach presents serious reliability flaws, commonly related to heat management challenges that ultimately shorten the lifetime of the driver. The reliability problem is further enhanced by the fact that the cost of the technology used to build the converter is still considered a top priority. Therefore, most commercial LED lighting systems are still built from cheap, but less reliable components, aiming to keep these technologies affordable [35]. Centralised LED drivers allow to partially overcome the abovementioned drawbacks. The adoption of centralised LED driving solutions greatly simplifies the replacement of a faulty component in the driver, on the one hand, and boosts the potential of full exploitation of the driver capabilities. DC–DC converters based on the SIMO architecture are serious candidates to fulfil the requirements of centralised LED driving solutions [36], [37]. The SIMO architecture typically consists of a front-end converter, which develops the current control function, and multiple channels, responsible for implementing the dimming and, whenever applicable, the time-sharing functions. This driver configuration has certain advantages over single-channel LED drivers, namely the potential to decentralise the driver and the optimised utilisation of resources.

Given the comprehensive set of LED drivers with potential interest, it is important to define the most important requirements that should be met. Following paragraphs list and describe the requirements that reveal more critical to take into account in LED lighting applications.

LEDs are particularly susceptible of reproducing temporal light artifacts (TLAs). TLAs consist of undesired changes in the perception of light, caused by fluctuations over time of either luminance or spectral distribution. Indeed, TLAs seriously endanger the health of inhabitants, in the long term, reason why it is critical to deploy measures suitable to cancel out such threat. TLAs may take the form of flicker, phantom arrays or stroboscopic effects [38]. Flicker is perhaps the most common and critical TLA linked to LED lighting technologies. The presence of flicker in LED lighting systems usually finds its roots on either the power supply or the power converter. It typically arises from fluctuations on the source voltage or other sources of noise, control signals introduced in the electricity distribution grids [39], or even failure of particular components of the converter. In the framework of this study, emphasis is put into the study of DC–DC converters. Hence, concerns are directed into the elimination of the phenomena responsible for TLAs whose roots are located in the power converter. Elimination of noise through proper selection of filters, along with the integration of fault tolerance strategies, are two desirable features to consider for the selected LED drivers.

Lighting systems found in homes and offices usually consist of multiple strings and points of light emission. Current regulation must be provided to each of those strings. To

achieve such objective, two distinctive approaches may be adopted with regards to the positioning of the LED drivers. In case that LEDs and the corresponding power converters are placed nearby, it is said that a decentralised architecture is considered. On the other hand, it is said that a LED lighting system has a centralised architecture in case that the LEDs and the power electronics used to control them are place far apart. From the points of view of fault management and optimisation of resources, centralised LED lighting systems provide advantages, allowing to control multiple strings with power converter(s) placed in a central, easy-to-access unit. Besides, the adoption of a centralised architecture opens up the possibility to control all LED strings with a single power converter, composed of multiple outputs.

Cost is, naturally, another concern to address in the selection of LED drivers. Thanks to the reduction on the number of components required for its implementation, solutions based on centralised LED drivers provide advantages over the decentralised ones in this regard.

According to the set of requirements listed above, this work addresses LED lighting systems based on three architectures: the architecture based on multiple non-isolated buck converters; the one based on the original SIMO converter, as proposed in [39]; and the architecture based on the fault-tolerant SIMO converter. All three converters are arranged in a way to allow the concurrent supply of multiple LED strings. Current control functions are deployed on both systems, resorting to analogue and pulse width modulation (PWM) dimming. These are the three converter topologies capable of better fulfilling the

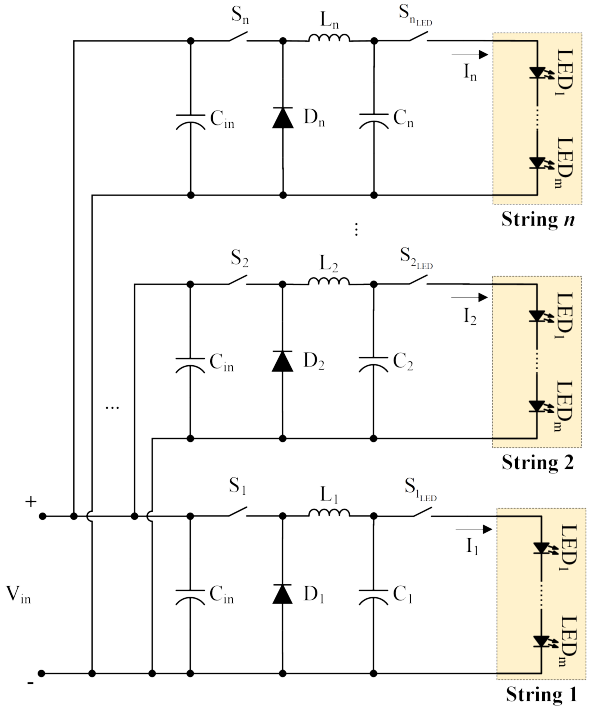


Fig. 3.3 Multi-output LED lighting system based on the buck converter.

requirements of LED lighting applications targeted at homes and offices, based on the judgement to the criteria enumerated above.

Fig. 3.3 depicts the structure of a multi-string LED lighting system supplied by multiple buck converters, adapted to the requirements of LED lighting applications.

Fig. 3.4 depicts the structure of a LED lighting system adopting a SIMO converter. It is noted that this is the conventional architecture of the SIMO converter, i.e., the architecture of the converter adopted as the root for the contributions made in this work in the field of LED lighting.

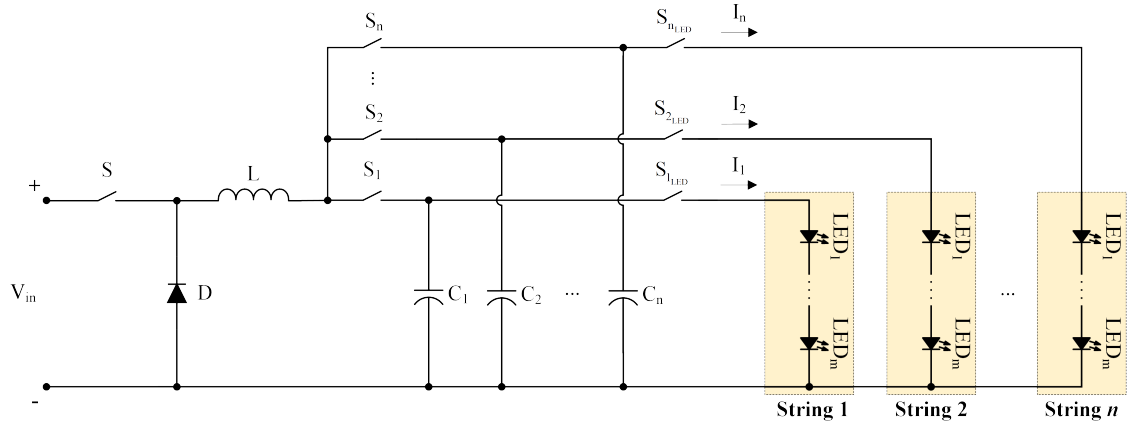


Fig. 3.4 Multi-output LED lighting system based on the SIMO converter.

From now on, attention is focused on the novel, fault-tolerant SIMO converter, as represented in Fig. 3.5. Because of its relevance in the context of this thesis, the analysis of the principles of operation will be entirely focused on this converter architecture.

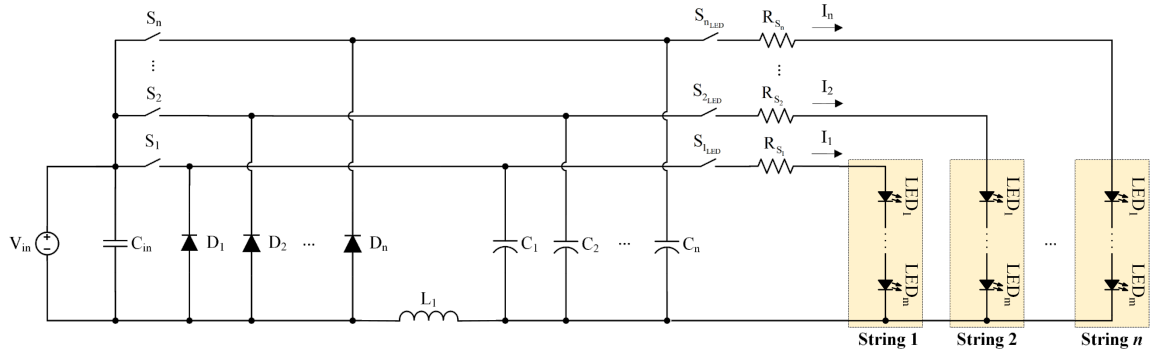


Fig. 3.5 Multi-output LED driver based on the fault-tolerant SIMO converter.

The converter is composed of *n* channels, each of them supplying *n* identical LED strings. It results from the improvement of the SIMO LED driver presented in [36]. With such upgrade, benefits like optimised utilisation of components and fault tolerance capability are introduced.

Switches S_1 ... S_n develop both current control and time-sharing functions, while switches $S_{1_{LED}}$ ... $S_{n_{LED}}$ develop the dimming functions. Resistors R_{S_1} ... R_{S_n} act as current

sensors, transducing currents I_1 ... I_n into voltages, which are then used to provide information for the current control loops.

Note that the converter depicted in Fig. 3.5 may include additional channels, allowing to connect several LED strings in the same driver. The scalability of the LED driver enhances the potential to fully exploit the resources available in the driver, namely the passive components. Besides, it assures minimal degradation on the quality of the light produced by the LED strings, in the event of failure on the converter.

3.2.1. Fault-tolerant SIMO converter – control strategy

Fig. 3.6 provides a schematic representation of the implemented controller, responsible for concurrently deploying the current control, time-sharing and dimming functions. The depicted structure is employed for one channel of the driver, meaning that the controller must be replicated according to the number of LED strings connected to the driver. Just like the converter, the controller has a scalable structure, which greatly simplifies the process of expansion of the driver into multiple LED strings. The principles of implementation of the controller result from the improvement of those proposed in [36].

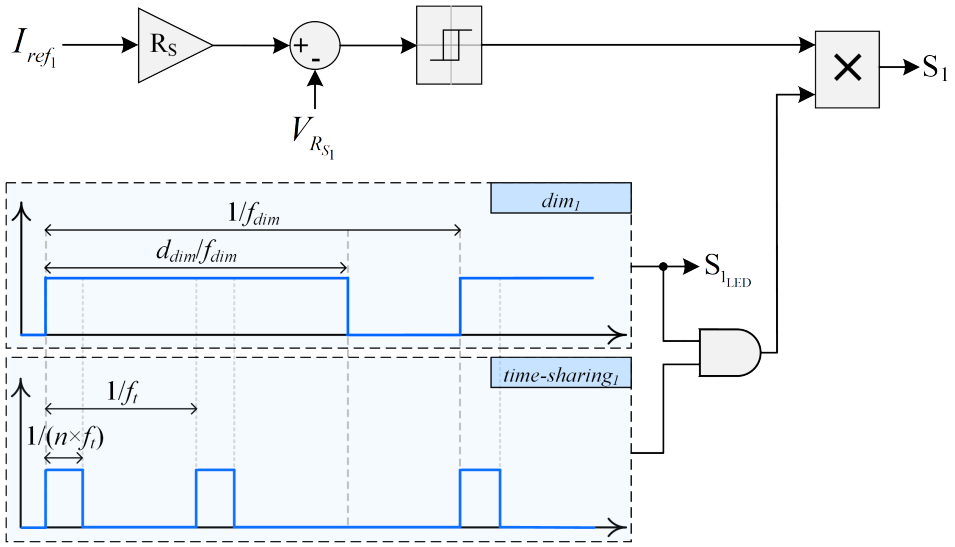


Fig. 3.6 Simplification of the control structure used to perform the current control, time-sharing, and dimming functions, for each LED driver channel.

The dimming command dim_1, with a frequency f_{dim} and duty ratio d_{dim}, is directly sent to the dimming switch $S_{1_{LED}}$. The features of the command dim_1 are identical to those of any other dimming signal. The ratio d_{dim} is controlled to obtain the desired luminous flux, so that the average current flowing through each LED string is changed accordingly. A second command signal, denoted as $time\text{-}sharing_1$, introduces the time-sharing function. This signal has a frequency f_t, higher than the dimming frequency f_{dim}, and a constant duty ratio of $1/n$, where n denotes the number of LED strings connected to the driver. The function of

this signal is to assign equal time slots to all the LED strings, over a period $1/f_t$. In practice, the higher the number of LED strings connected to the driver, the smaller is the time slot assigned to each LED string. This feature enables the exploitation of the entire dimming range.

The structure of the implemented current controller is quite simple yet effective, as requested for any residential lighting system. A closed-loop current controller, based on a sliding-mode controller, is implemented. For improved accuracy in the control of the string current, the current flowing through string 1 I_1 is translated by resistor R_{S_1} into the voltage $V_{R_{S_1}}$, fed into the current controller. Identical procedure is adopted to provide the controller with the reference value: the reference current I_{ref_1} is translated into voltage by applying the gain R_S.

The logical AND operation of the command signals dim_1 and $time\text{-}sharing_1$ defines the periods of time at which the current controller should drive switch S_1. The multiplication operand integrates the result of the logical AND operation into the current controller.

Fig. 3.7 provides an overview of the switching pattern implemented to control the switches $S_{1_{LED}} \dots S_{n_{LED}}$, responsible for the dimming functions. The principles of implementation of this low-frequency switching pattern are equal to those used in interleaved DC–DC converters. Each dimming command is shifted by $2\pi/n\ rad$ between each other, with n denoting the number of converter outputs. Referring to Fig. 3.7, it is possible to observe that each dimming signal has a duty ratio equal to d_{dim} and period of T_{dim} $\left(T_{\text{dim}} = 1/f_{\text{dim}}\right)$. For compactness and intelligibility, only the most representative tick labels are inserted in the time axis of Fig. 3.7.

It is also important to note that, thanks to the merits of the adopted modulation strategy, the dimming range is extended and, consequently, the duty ratio of the dimming commands can be set within the [0 1] interval.

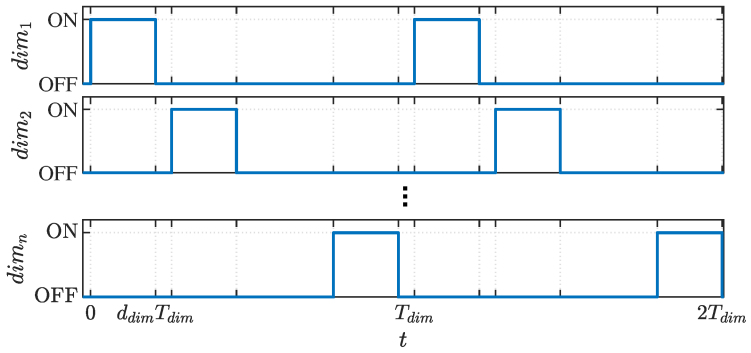


Fig. 3.7 Generic representation of the switching pattern implemented to drive switches $S_{1_{LED}} \dots S_{n_{LED}}$.

Fig. 3.8 provides a general picture on the switching pattern of switches $S_1 \dots S_n$, responsible for developing the current control and time-sharing functions. Notice that there is a superposition in time of the switching commands with dimming functions $dim_1 \dots dim_n$,

depicted in Fig. 3.7, and the switching commands provided to switches S_1 … S_n, depicted in Fig. 3.8. In practice, this implies that switches S_1 … S_n can only be active when the corresponding dimming switches are also active. Taking a closer look at the command signal of switch S_1, it is possible to distinguish two frequency components: a medium-frequency component, related to the time-sharing function, which is imposed by the command signal *time-sharing*$_1$; and a high-frequency component, related to the current control function, which is imposed by the sliding-mode controller.

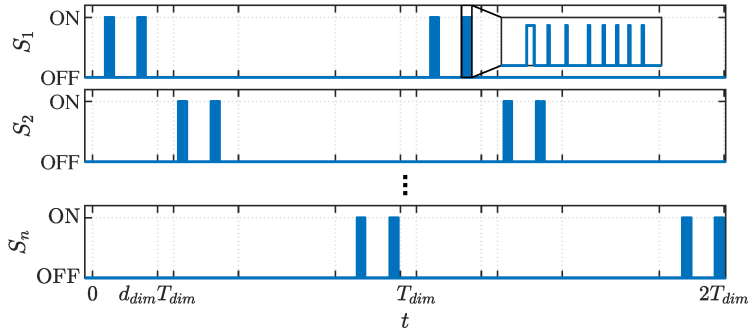


Fig. 3.8 Generic representation of the switching pattern implemented to drive switches S_1 … S_n, including a zoomed view of signal S_1.

As a result of the implementation of the presented control strategy, the current measured at each output of the LED driver is not constant over time. Instead, each LED string is supplied by a square current waveform, with duty ratio equal to d_{dim} and frequency equal to f_{dim}. Thanks to the architecture of the control strategy, the amplitude of the square waveform is also controllable and can be easily adjusted. Hence, the dimming function can be concurrently ensured through PWM dimming and analogue dimming.

As widely demonstrated in the literature, it is important that the dimming frequency remains above a certain threshold, so that human beings are not subjected to undesirable and hazardous perceivable flicker – most widely accepted low threshold is 300 *Hz* [40]. Still, some references opt by higher dimming frequencies [37], aiming to eliminate the risk of perceivable flicker.

3.3. EV charging

The uptake of e-mobility, considered one of the most sustainable and promising mobility solutions for the coming years, is conditioned by a set of factors, being the deployment of a broad charging infrastructure considered the pivotal one [41]. Apart the relevance of a broad public charging infrastructure, it is equally relevant to provide all necessary tools and incentives for the implementation of private charging points, installed at homes and offices, given the fact that EVs spend most of the time parked next to these two types of facilities. Besides, the preference of EV users typically falls upon homes and

offices when it comes to charging their vehicles. Indeed, such preference is already reflected in the energy consumption profiles of many homes and offices. EV charging already stands out as one of the most representative energy consuming applications of homes and offices. The potential of growing related to EV charging services in the near future makes the study of this application even more relevant. In addition, statistical studies reveal that, within the broad range of research domains strictly linked to EVs, the domain of charging procedures and technologies is among the ones that are less mature at the moment, but at the same time among the ones that receive more research interest, with multiple contributions being made lately [42].

Following paragraphs list and describe the requirements that reveal more prominent and important to take into account in the development of EV charging solutions entirely supported through DC–DC converters.

The fairly high power levels required by such application imply the adoption of power conditioning solutions based on DC–DC converters capable of handling high voltage and current ratings, in order to support the adoption of EV charging services complying with the requirements of DC microgrids. To address the challenges presented by high-power applications, converter topologies featuring modular architecture are usually considered a good option. By splitting the processed power into multiple modules/components, it is possible to strongly alleviate the stress imposed to the components, on the one hand, and to reduce the overall ratings of those components, making them cheaper and smaller.

Another important criterion to consider is related to power quality. Supplying energy with voltage and current ripple are important factors promoting overheating and loss of lifetime on batteries [43]. Hence, it is pivotal that the power converters considered for EV charging applications provide all means to ensure strict voltage and current regulation at the output of the EV charger, even under a multitude of scenarios with potential to perturb the effective operation of the EV charging operation. Faults in the power converter are perhaps the most recurring events introducing severe and unforeseen perturbations on the power quality. The adoption of fault-tolerant converters and effective reconfiguration strategies, suitable to overcome the negative effects of faults, are commonly considered to address the challenges posed by faults. Other power quality issues shall be dealt with proper design of the converter filters, along with the adoption of advanced control strategies, as it is the case of model predictive control [44].

Traditional EV chargers are usually complex, making their acquisition by private owners and domestic consumers fairly cost-prohibitive. On that basis, the selection of the DC–DC converters should consider the cost of implementation associated to them. With regards to cost/complexity, it is possible to establish a distinction between non-isolated and isolated DC–DC converters. Because of the higher number of active and passive components

required to build isolated DC–DC converters, these converters also tend to imply higher costs of acquisition [45]. Hence, non-isolated DC–DC converters reveal advantageous with regard to cost.

The demand for enhanced smartness in the charging procedures reveals fundamental to ensure the sustainable deployment of a large-scale charging infrastructure [41]. One of the key enablers of smarter charging is strictly related to the capability of EV chargers to provide bidirectional power flow. This is a critical enabler of vehicle-to-grid (V2G) services, which are expected to become commonplace in the near future, also in the context of homes and offices.

In the literature, reactive power regulation is mentioned as another critical feature of EV chargers [46]. Such concern is commonplace because of the prevalence of AC power systems. Since DC microgrids are the focus of this work, such concern is not placed in the systems under evaluation, thanks to the architecture of the power system, based on DC energy.

Based on the set of requirements listed above and on the evaluation of candidate converter topologies, this work adopts the non-isolated bidirectional interleaved converter and the non-isolated bidirectional multilevel converter as the subject of study for EV charging applications. These are the two converter topologies capable of better fulfilling the requirements of domestic EV charging applications, based on the judgement to the criteria enumerated above.

Fig. 3.9 depicts the structure of a three-phase interleaved bidirectional DC–DC converter, considered in this work. It is the result of the connection, in parallel, of three simple non-isolated bidirectional DC–DC converters. The selection of the number of phases is based on a careful evaluation and weighting between complexity of the converter, cost, and power ratings to handle.

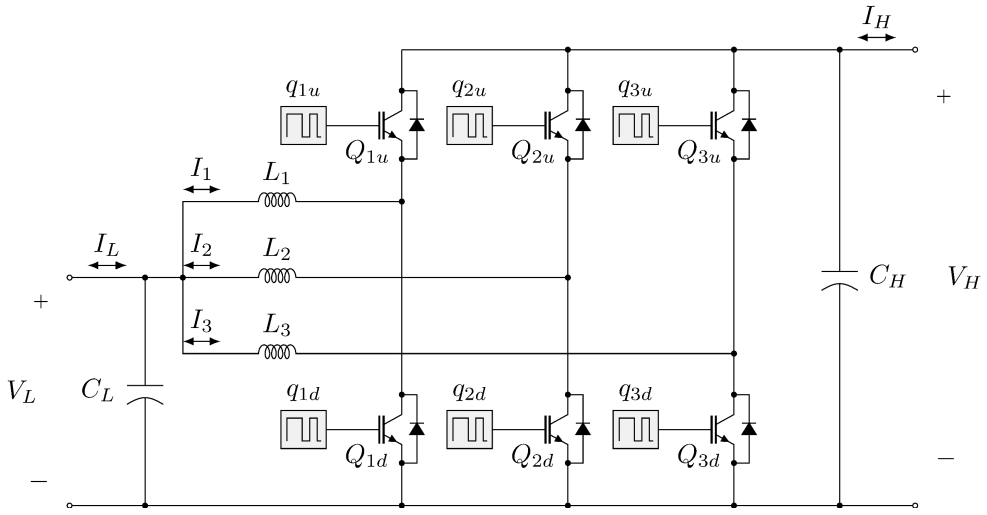


Fig. 3.9 Three-phase interleaved bidirectional DC–DC converter.

Fig. 3.10 depicts the structure of a three-level bidirectional DC–DC converter, considered in this work for EV charging applications. It is the result of the connection, in series, of two simple non-isolated bidirectional DC–DC converters. The denomination of the converter finds its roots on the number of voltage levels which the converter can provide at its output. For the three-level converter, and according to the nomenclature adopted in Fig. 3.10, the high-voltage side may assume the voltage levels {0 V_H/2 V_H} V. Just like for the interleaved converter, the selection of the number of converter levels is based on a careful evaluation and weighting between complexity of the converter, cost, and power ratings to handle.

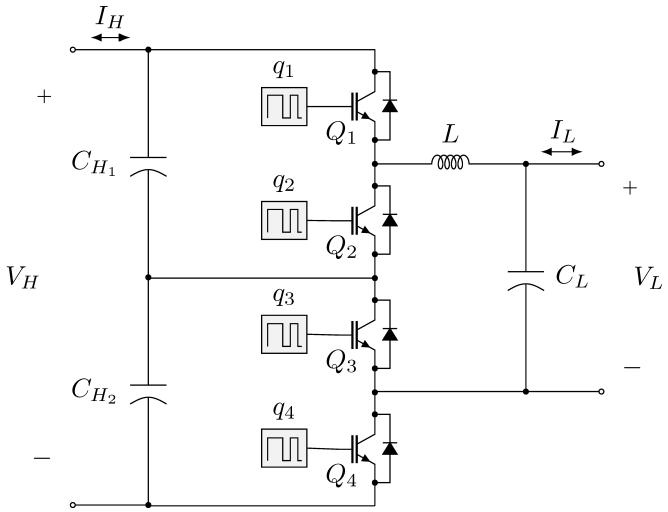


Fig. 3.10 Three-level bidirectional DC–DC converter.

3.3.1. Non-isolated interleaved bidirectional converter – control strategy

Given the similarity between the interleaved bidirectional converter and the interleaved unidirectional converter, in terms of architecture and principles of operation, it is also possible to employ a strategy based on the average current control, taking into consideration some adaptations. For the unidirectional converter, the main objective consists of the regulation of the converter output voltage V_{out}. As for the bidirectional converter, the main objective consists of the regulation of the low-voltage side current I_L, since EV charging applications commonly opt by control strategies based on current regulation. On that basis, the number and configuration of the control loops imply modifications.

To effectively accomplish the average current control, the controlled variable (I_L) is sampled in precise instants, being the process of sampling synchronised resorting to the triangular carriers produced in the PWM modulator. The single output of the current regulator provides the switching duty cycle d, to be introduced in the PWM modulator.

Note that the PWM modulator outputs only three distinctive PWM signals, sent to the gates of the power switches. Depending on the operation mode (boost mode or buck mode), the three gating signals are routed to two distinctive groups of power switches. In other words, the gating signals are sent to switches Q_{1d}, Q_{2d}, and Q_{3d} – refer to Fig. 3.9 – when the converter is operated in boost mode; on the other hand, the gating signals are sent to switches Q_{1u}, Q_{2u}, and Q_{3u} – refer to Fig. 3.9 – when the converter is operated in buck mode.

Fig. 3.11 shows the architecture of the adopted average current control strategy.

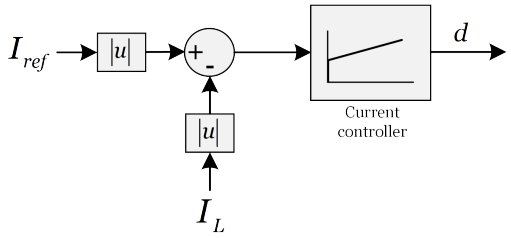


Fig. 3.11 Simplification of the control structure of the non-isolated bidirectional interleaved converter.

The parameters of the PI controller are compiled in Table 3.3.

TABLE 3.3 CONTROLLER PARAMETERS

Parameter	Value
K_p	0.1
K_i	0.8

3.3.2. Non-isolated bidirectional multilevel converter – control strategy

Multilevel DC–DC converters have a particular architecture and, consequently, imply the adoption of control strategies with distinctive features. Given the application under consideration (EV charging), current control is preferable.

Fig. 3.12 shows the architecture of the adopted control strategy.

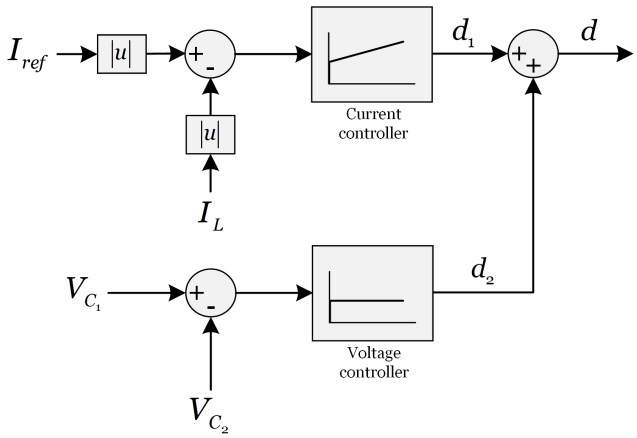


Fig. 3.12 Simplification of the control structure employed in the non-isolated bidirectional multilevel converter.

The current controller monitors and acts on the low-voltage side current I_L – refer to the circuit of the multilevel converter depicted in Fig. 3.10. Current control is developed through the implementation of a PI controller, whose parameters are compiled in Table 3.4.

Apart the current control function, the multilevel converter shall also ensure continuous balance between the two capacitor voltages, denoted as V_{C_1} and V_{C_2} – refer to the circuit of the multilevel converter depicted in Fig. 3.10. The balance of the two voltages is assured through a P controller, inserted in parallel with the current controller. The parameters of the P controller are listed in Table 3.5.

The duty cycle d to be effectively sent to the PWM modulator results from the sum of the two controllers: the PI controller assuring current control and the P controller assuring voltage control.

Note that the PWM modulator outputs two distinctive gating signals, shifted by $\pi/2$ *rad* between each other. Depending on the operation mode (boost mode or buck mode), the two gating signals are routed to two distinctive groups of power switches. In other words, the gating signals are sent to switches Q_2 and Q_3 – refer to Fig. 3.10 – when the converter is operated in boost mode; on the other hand, the gating signals are sent to switches Q_1 and Q_4 – refer to Fig. 3.10 – when the converter is operated in buck mode.

Just like other converter topologies employing average current control, the controller of the multilevel converter samples the controlled variables (I_L, V_{C_1} and V_{C_2}) in precise instants, being the sampling process synchronised resorting to the triangular carriers produced in the PWM modulator.

The parameters of the current and voltage controllers are compiled in Table 3.4 and Table 3.5.

TABLE 3.4 CURRENT CONTROLLER PARAMETERS

Parameter	Value
K_p	0.8
K_i	10

TABLE 3.5 VOLTAGE CONTROLLER PARAMETERS

Parameter	Value
K_p	0.8
K_i	0

Chapter 4

Operation principles of DC–DC converters: healthy and faulty operation

The complete understanding about the typical failure mechanisms of power converters is an essential step towards the development of fault diagnostic strategies which, in turn, help improving the availability and resilience of power converters. OC faults are among the most common failure modes on power electronics converters and, at the same time, the ones that show tremendous impact on the converters' operation.

Following sections provide an extensive theoretical evaluation of the converters' operation principles, under healthy and faulty conditions, aiming to understand the impact of faults on the operation of the converters considered in this study. Based on the comparison between healthy and faulty operation, it becomes possible to identify potential fault signatures, fundamental to assure accurate fault diagnostics. Emphasis is put into the analysis of the non-isolated unidirectional interleaved boost converter and of the fault-tolerant SIMO converter, considered the two topologies with more relevance in the context of this work. It is worth noting that the principles of operation of the unidirectional interleaved boost converter are extensible to the bidirectional interleaved converter, when operated in boost mode.

4.1. General appliances

4.1.1. Non-isolated unidirectional interleaved boost converter

4.1.1.1. Operation principles under healthy condition

The following analysis aims the evaluation of the three-phase non-isolated unidirectional interleaved boost converter, depicted in Fig. 3.1. The converter input current comprises the sum of each phase current:

$$I_{in} = \sum I_n = I_1 + I_2 + I_3 \tag{4.1}$$

Based on (4.1), the derivative of the converter input current dI_{in}/dt comprises the sum of the derivatives of each phase:

$$\frac{dI_{in}}{dt} = \sum \frac{dI_n}{dt} = \frac{dI_1}{dt} + \frac{dI_2}{dt} + \frac{dI_3}{dt} \tag{4.2}$$

Taking into account the identical nature between converter phases, an analysis will be performed for just one converter phase. When the power switch Q_1 is conducting, the derivative of the inductor current dI_1 / dt is given by:

$$\frac{dI_1}{dt} = \frac{V_{in}}{L_1} \tag{4.3}$$

Meanwhile, when the switch is off, the derivative of the current flowing through the inductor dI_1 / dt is given by:

$$\frac{dI_1}{dt} = \frac{V_{in} - V_{out}}{L_1} \tag{4.4}$$

Considering the ideal model of the interleaved boost converter, the voltage gain of the interleaved boost converter is expressed as follows:

$$\frac{V_{out}}{V_{in}} = \frac{D_M}{D_M - D} \tag{4.5}$$

where D_M denotes the period of non-zero inductor current and D denotes the switching duty cycle.

Assuming equal components in all the converter phases, it is possible to derive the general expressions of the input current derivative, for each interval of a switching period, based on (4.2)–(4.5). Intervals are defined and delimited taking into account the number of converter switches which are simultaneously active. Particular attention is given to the intervals that have the maximum number of switches simultaneously in ON-state. As it will be demonstrated further ahead, these are the intervals of interest for the implementation of the fault diagnostic strategies. Fig. 4.1 highlights the intervals of interest for the analysis of the converter operation, for the different ranges of duty cycle D. All intervals begin with a rising edge of any of the three PWM signals and finish with the subsequent falling edge occurring in the switching pattern.

The following theoretical analysis, valid for both DCM and CCM, will solely focus on the intervals highlighted in Fig. 4.1.

For ease of analysis, the following assumptions are taken:

1) Considering the converter steady-state condition, it is possible to assume that variables D and D_M do not suffer significant oscillations along one switching period and, consequently, these variables remain constant.

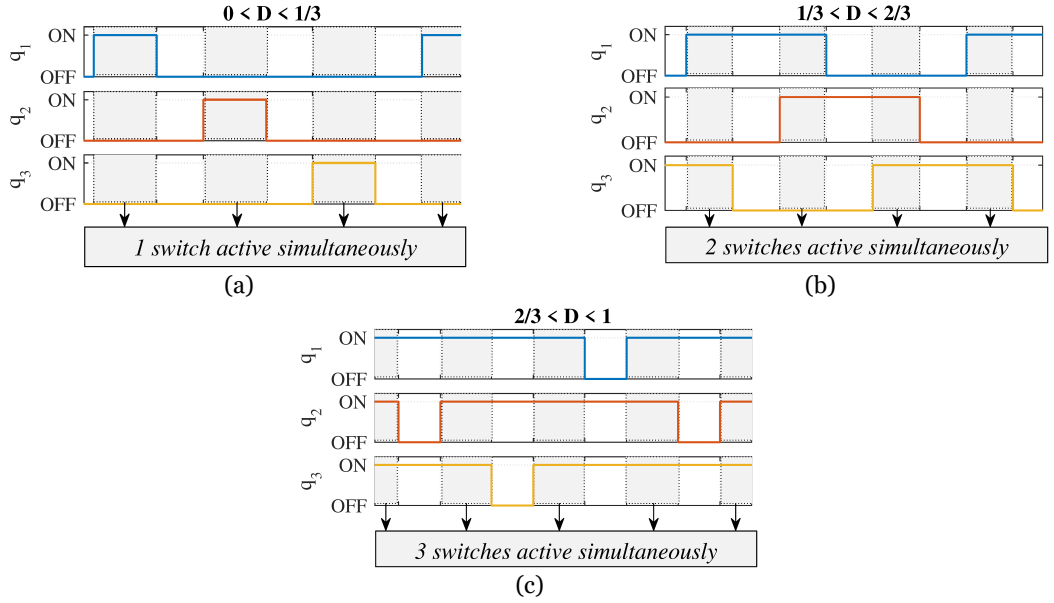


Fig. 4.1 Converter switching patterns and intervals of interest for the analysis of the converter operation, considering three distinctive ranges of switching duty cycle: (a) $D < 1/3$; (b) $1/3 < D < 2/3$; (c) $2/3 < D < 1$.

2) D_M is always equal or higher than D. In practice, this means that condition $D_M - D$ is always positive.

Based on the aforementioned assumptions, the information of the derivative of I_{in} (dI_{in}/dt), expressed in Table 4.1, provide useful information about the evolution trend of I_{in} for the intervals highlighted in Fig. 4.1, under healthy converter operation.

TABLE 4.1 INPUT CURRENT DERIVATIVE FOR THE INTERVALS WITH THE MAXIMUM NUMBER OF ON-STATE SWITCHES

D	D_M	N^*	dI_{in}/dt
$0<D<\frac{1}{3}$	$0<D_M<\frac{1}{3}$	1	$\frac{V_{in}}{L}>0$
	$\frac{1}{3}<D_M<\frac{2}{3}$	1	$\frac{V_{in}}{L}>0$
		2	$\frac{(D_M-2D)V_{in}}{(D_M-D)L}>0$
	$\frac{2}{3}<D_M<1$	2	$\frac{(D_M-2D)V_{in}}{(D_M-D)L}>0$
		3	$\frac{(D_M-3D)V_{in}}{(D_M-D)L}>0$
$\frac{1}{3}<D<\frac{2}{3}$	$\frac{1}{3}<D_M<\frac{2}{3}$	2	$\frac{2V_{in}}{L}>0$
	$\frac{2}{3}<D_M<1$	2	$\frac{2V_{in}}{L}>0$
		3	$\frac{(2D_M-3D)V_{in}}{(D_M-D)L}>0$
$\frac{2}{3}<D<1$	$\frac{2}{3}<D_M<1$	3	$\frac{3V_{in}}{L}>0$

*Nomenclature: N - Number of converter phases with non-zero current.

Based on the data provided on Table 4.1, it is concluded that, under healthy converter operation, I_{in} increases in the intervals highlighted in Fig. 4.1, regardless of the values assumed by variables D and D_M.

4.1.1.2. Operation principles under OC fault condition

The proper operation of non-isolated unidirectional interleaved boost converters becomes seriously affected in the presence of failures on the active switches of the converter. A single OC fault has potential to completely shut down one phase of the converter.

After an OC fault in an active switch, no current flows through it. As a result, the phase current will decrease linearly, reaching zero phase-current soon. Analytically, the derivative of the current flowing through the inductor dI_1 / dt, measured within the period comprised between the OC fault and the moment in which the phase current reaches zero, is given by:

$$\frac{dI_1}{dt} = \frac{V_{in} - V_{out}}{L_1} \tag{4.6}$$

Based on (4.6), the derivative of the current flowing through the faulty phase becomes temporarily negative. As the derivative of I_{in} is a result of the sum of the derivatives of the individual phase currents (dI_1/dt, dI_2/dt, and dI_3/dt), the impact of OC faults will also impact the evolution of the I_{in} derivative.

Taking the assumptions made when evaluating the operation principles of the converter under healthy condition – refer to Section 4.1.1.1, it is possible to derive the expressions of the I_{in} derivative, now considering a scenario of OC fault. Table 4.2 compiles information about the derivative of I_{in}, computed in the presence of an OC fault in the insulated gate bipolar transistor (IGBT) Q_1. Note that the last column of Table 4.2 includes labels for better identification of each scenario. The information about the I_{in} derivative provided in Table 4.2 is computed through the evaluation of I_{in} along the intervals of the switching pattern starting at the rising edge of the PWM signal q_1. Such intervals are highlighted in Fig. 4.2, for each of the three possible ranges of duty cycle.

More important than the magnitude assumed by the I_{in} derivative, it is relevant to support the analysis of the converter condition on the signal of the I_{in} derivative instead. Based on the data provided in Table 4.2, it is concluded that the I_{in} derivative becomes negative after the OC fault for most scenarios. An exception to this statement is verified in two scenarios. The I_{in} derivative is positive when variables D and D_M are within the same range of variation, as soon as the steady-state condition is recovered – scenarios (g) and (k)

TABLE 4.2 INPUT CURRENT DERIVATIVE UNDER AN OC FAULT SCENARIO

D	D_M	N^*	dI_{in}/dt
$0<D<\frac{1}{3}$	$0<D_M<\frac{1}{3}$	0	0 (a)
		1	$(-DV_{in})/((D_M-D)L)<0$ (b)
	$\frac{1}{3}<D_M<\frac{2}{3}$	1	$(-DV_{in})/((D_M-D)L)<0$ (c)
		2	$(-2DV_{in})/((D_M-D)L)<0$ (d)
	$\frac{2}{3}<D_M<1$	2	$(-2DV_{in})/((D_M-D)L)<0$ (e)
		3	$(-3DV_{in})/((D_M-D)L)<0$ (f)
$\frac{1}{3}<D<\frac{2}{3}$	$\frac{1}{3}<D_M<\frac{2}{3}$	1	$V_{in}/L>0$ (g)
		2	$((D_M-2D)V_{in})/((D_M-D)L)<0$ (h)
	$\frac{2}{3}<D_M<1$	2	$((D_M-2D)V_{in})/((D_M-D)L)<0$ (i)
		3	$((D_M-3D)V_{in})/((D_M-D)L)<0$ (j)
$\frac{2}{3}<D<1$	$\frac{2}{3}<D_M<1$	2	$2V_{in}/L>0$ (k)
		3	$((2D_M-3D)V_{in})/((D_M-D)L)<0$ (l)

*__Nomenclature:__ ***N*** - Number of converter phases with non-zero current.

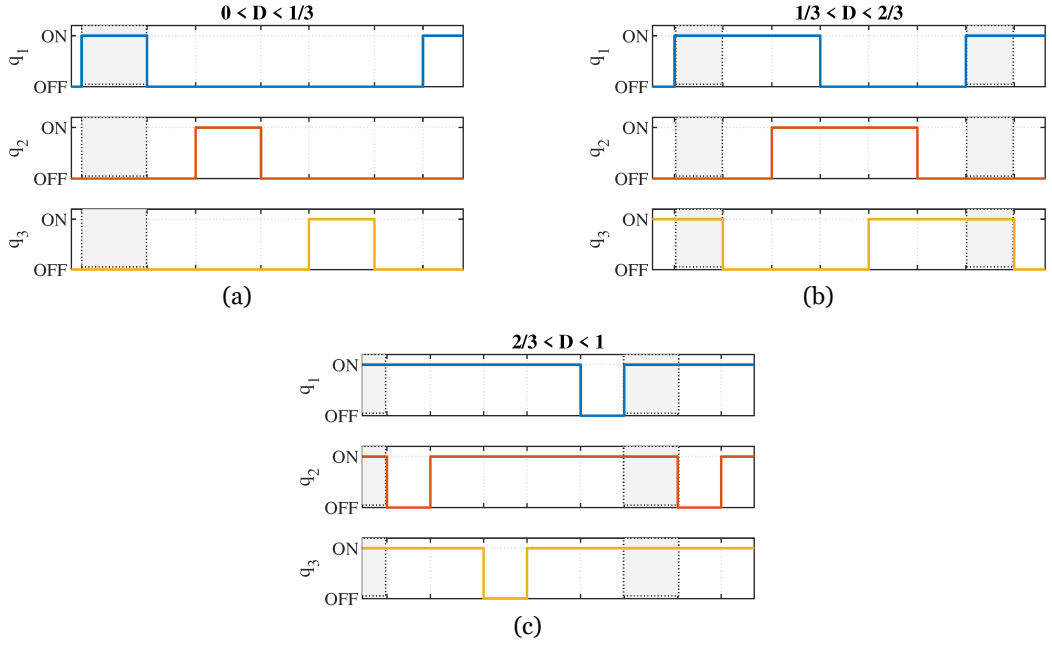


Fig. 4.2 Intervals of interest for the evaluation of the condition of IGBT Q_1, assessed through the derivative of the converter input current (dI_{in}/dt). The intervals of interest are established according to three distinctive ranges of duty cycle: (a) $D < 1/3$; (b) $1/3 < D < 2/3$; (c) $2/3 < D < 1$.

of Table 4.2. In general, these exceptions should not compromise the deployment of diagnostic strategies, since the I_{in} derivative is still negative for the transient state observed right after the fault – scenarios (h) and (l) of Table 4.2.

4.1.1.3. Simulation results

To confirm the theoretical formulation regarding the operation of the non-isolated unidirectional interleaved boost converter, under both healthy and OC fault conditions, a comprehensive set of operation scenarios was defined. Several levels were considered for the converter output voltage V_{out}, in order to address a wide range of duty cycle D values. Also, the switching frequency was varied to take into account any potential influence of the switching frequency on the response of the converter. Further details regarding the simulation model, its architecture and the parameters considered for the evaluation are provided in Appendix A.1.

In all simulated scenarios, OC fault conditions in IGBT Q_1 are considered.

Fig. 4.3 shows the most relevant converter input and output variables, assessed at an output voltage V_{out} of 42 V and switching frequency f_{sw} of 1 kHz.

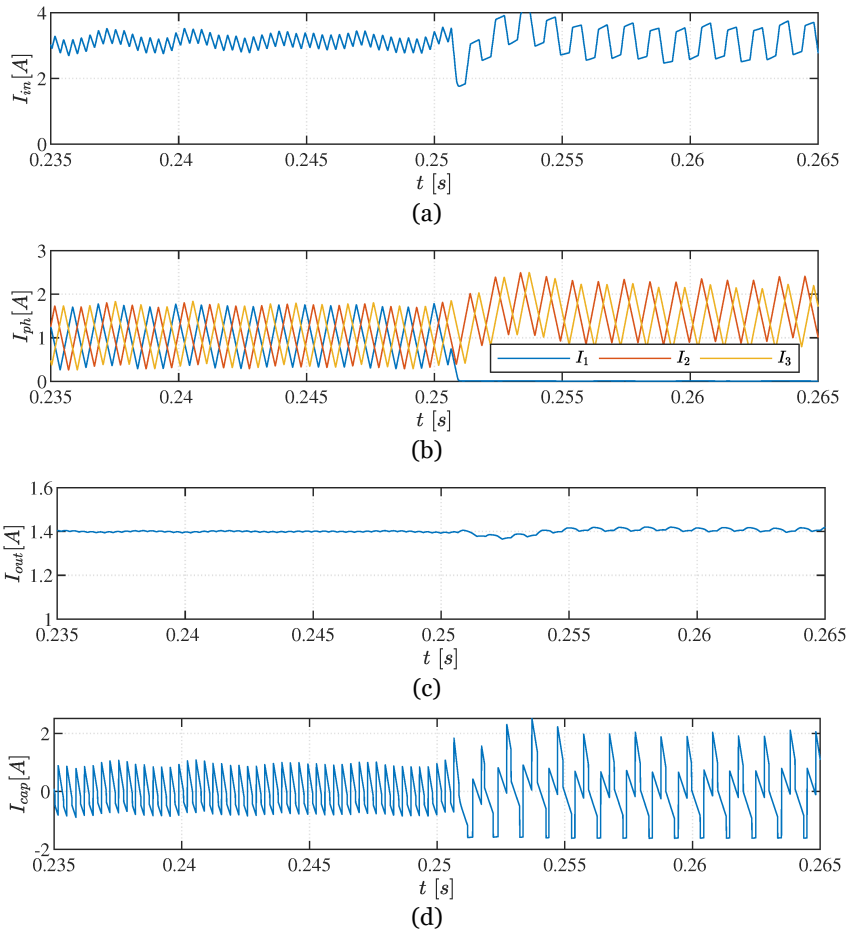


Fig. 4.3 Evolution, in time, of the most relevant converter variables: (a) Converter input current I_{in}; (b) Phase currents $I_{1...3}$; (c) Converter output current I_{out}; and (d) Output capacitor current I_{cap}. An OC fault occurs at t = 0.2501 s, in IGBT Q_1.

The results shown in Fig. 4.3 are framed into the condition of duty cycle $0 < D < 1/3$, with $D_M = 1$, as the converter operates in CCM.

Referring to the waveform of the input current I_{in} – Fig. 4.3 (a) – it is possible to observe the distinctive depreciation of the waveform right after the OC fault, in agreement with the mathematical condition defined in scenario (f) of Table 4.2. A temporary dip on the waveform is followed by increased ripple, which prevails over the post-fault steady state. The increased ripple on I_{in} is a result of the unbalanced switching pattern imposed to the converter phases that remain healthy. Referring to Fig. 4.3 (b), which depicts the converter phase currents, it is possible to notice the uneven temporal distribution of the phase currents, characteristic of an unbalance switching condition. The effects of such unbalance are also reflected on the output current I_{out} – Fig. 4.3 (c) – and capacitor current I_{cap} – Fig. 4.3 (d). As a consequence of the fault, it is also noted the increment of the phase currents from $1/3 \times I_{in}$ to $1/2 \times I_{in}$.

To evaluate the behaviour of the converter when the switching duty cycle is changed, a second scenario adopted another value for the output voltage. Fig. 4.4 shows the most

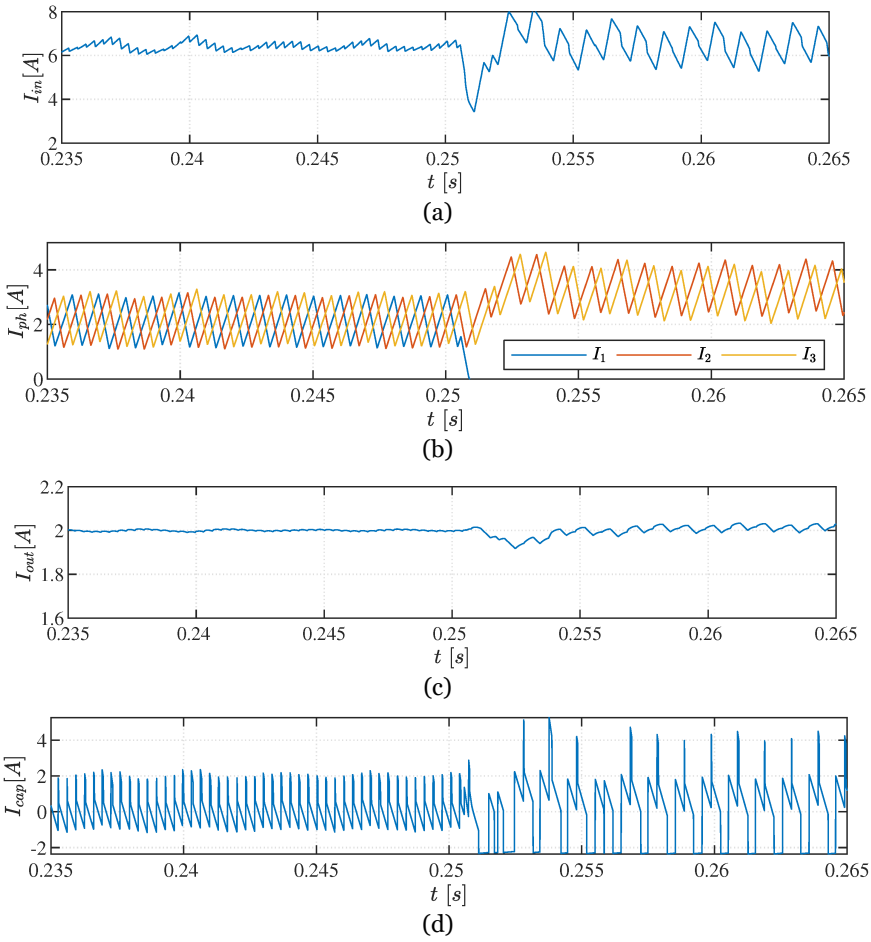


Fig. 4.4 Evolution, in time, of the most relevant converter variables: (a) Converter input current I_{in}; (b) Phase currents $I_{1...3}$; (c) Converter output current I_{out}; and (d) Output capacitor current I_{cap}. An OC fault occurs at $t = 0.2501\ s$, in IGBT Q_1.

relevant converter input and output variables, assessed at an output voltage V_{out} of 60 V and switching frequency f_{sw} of 1 kHz.

The results shown in Fig. 4.4 are framed into the condition of duty cycle $1/3 < D < 2/3$, with $D_M = 1$, since the converter operates in CCM. Referring to the waveform of the input current I_{in} – Fig. 4.4 (a) – it is possible to observe the distinctive depreciation of the waveform right after the OC fault, in agreement with the mathematical condition defined in scenario (j) of Table 4.2.

Despite the differences on the operation conditions, the results presented in Fig. 4.4 are pretty much aligned with those provided in Fig. 4.3. Only the order of magnitude of the variables changes, while the trends of evolution of the variables remain the same.

To understand how variations on the switching frequency impact the response of the converter to an OC fault, the third scenario considers a switching frequency f_{sw} equal to 3 kHz. Fig. 4.5 depicts the evolution of the converter variables, assessed at an output voltage V_{out} of 60 V and switching frequency f_{sw} of 3 kHz.

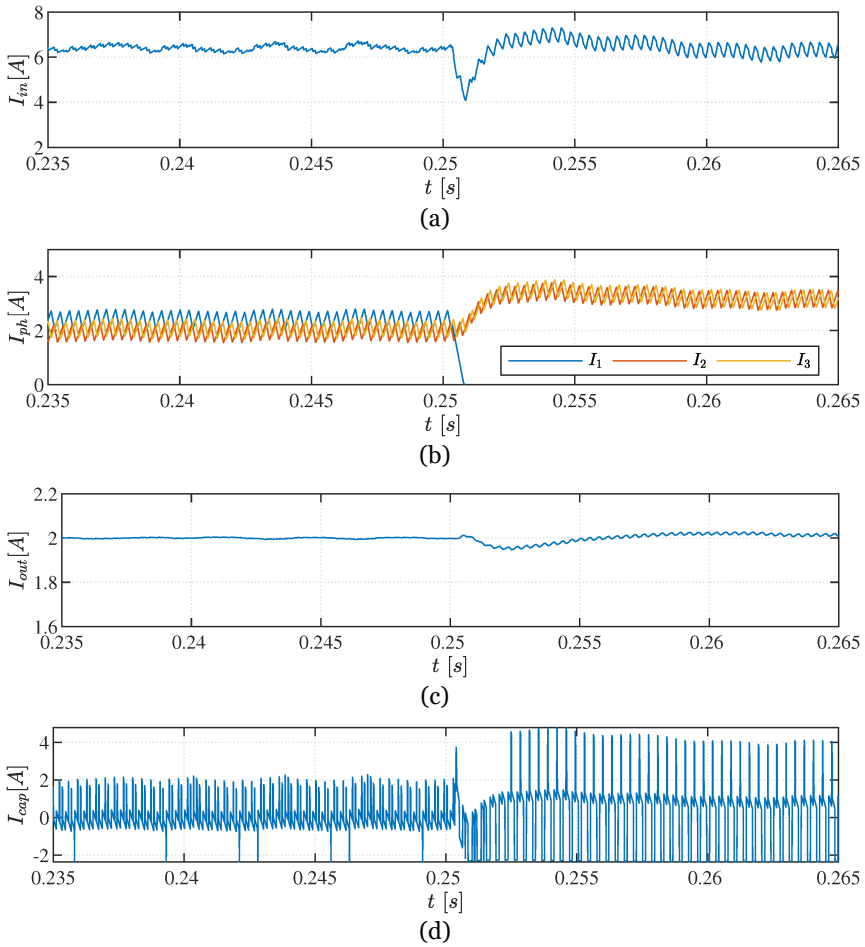


Fig. 4.5 Evolution, in time, of the most relevant converter variables: (a) Converter input current I_{in}; (b) Phase currents $I_{1...3}$; (c) Converter output current I_{out}; and (d) Output capacitor current I_{cap}. An OC fault occurs at t = 0.2501 s, in IGBT Q_1.

The results presented in Fig. 4.5 are also framed into the condition of duty cycle $1/3 < D < 2/3$, with $D_M = 1$. Thanks to the increment on the switching frequency, both the input current I_{in} and output current I_{out} reduce the order of magnitude of their ripples. Nevertheless, the sharp and provisional decay of the input current I_{in} prevails, allowing to easily identify an OC fault. Referring to the waveform of the input current I_{in} – Fig. 4.5 (a) – it is possible to observe the distinctive depreciation of the waveform right after the OC fault, in agreement with the mathematical condition defined in scenario (j) of Table 4.2.

4.1.1.4. Experimental results

Experimental tests were conducted to perform the validation of the simulation results. The scenarios adopted for the tests are identical to the ones considered in the simulations. Detailed information regarding the experimental setup, its architecture and the parameters considered in the tests are provided in Appendix B.1.

In all scenarios, OC fault conditions in IGBT Q_1 are considered.

Fig. 4.6 shows the most relevant converter input and output variables, assessed at an

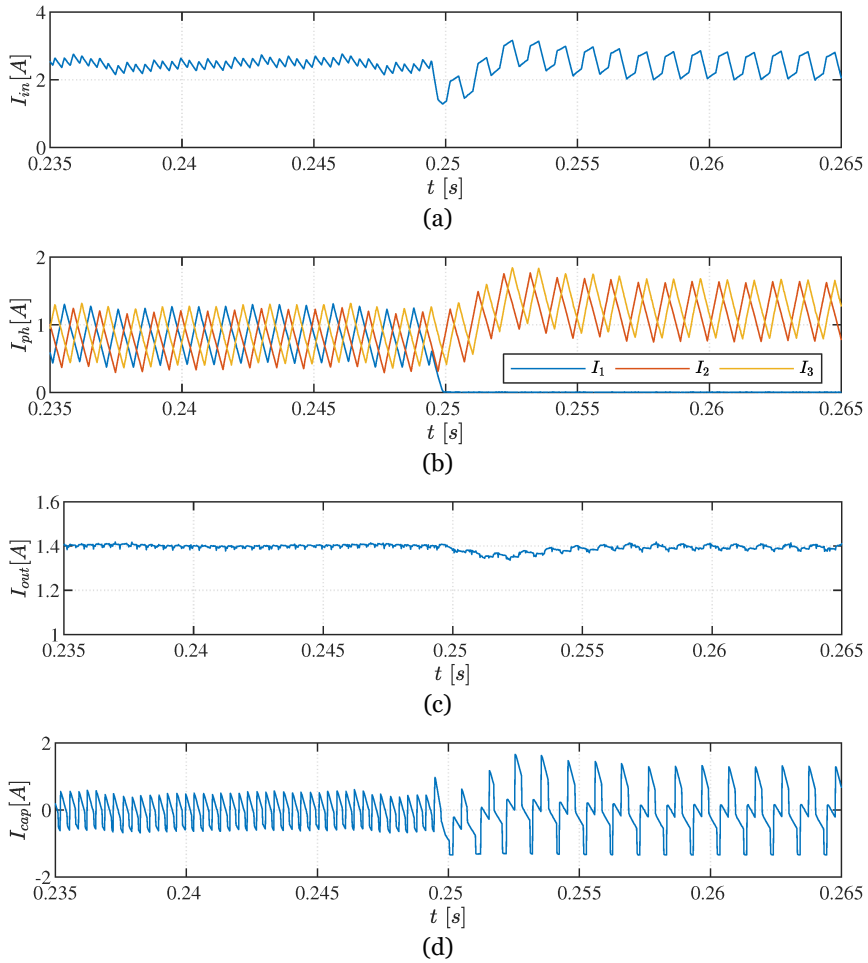


Fig. 4.6 Evolution, in time, of the most relevant converter variables: (a) Converter input current I_{in}; (b) Phase currents $I_{1...3}$; (c) Converter output current I_{out}; and (d) Output capacitor current I_{cap}. An OC fault occurs at $t = 0.2496\ s$, in IGBT Q_1.

output voltage V_{out} of 42 V and switching frequency f_{sw} of 1 kHz. The equivalent simulation results are provided in Fig. 4.3.

In general, all the variables show evolution patterns similar to the ones shown in simulation, for the corresponding scenario (Fig. 4.3), thus confirming the consistency of the results. Despite such consistency, it is possible to observe some expected low amplitude, high frequency white noise on the converter output current I_{out} – refer to Fig. 4.6 (c).

Fig. 4.7 depicts the waveforms of the most relevant converter variables, showing their evolution in the pre-fault and post-fault periods, assessed at an output voltage V_{out} of 60 V and switching frequency f_{sw} of 1 kHz. The equivalent simulation results are provided in Fig. 4.4.

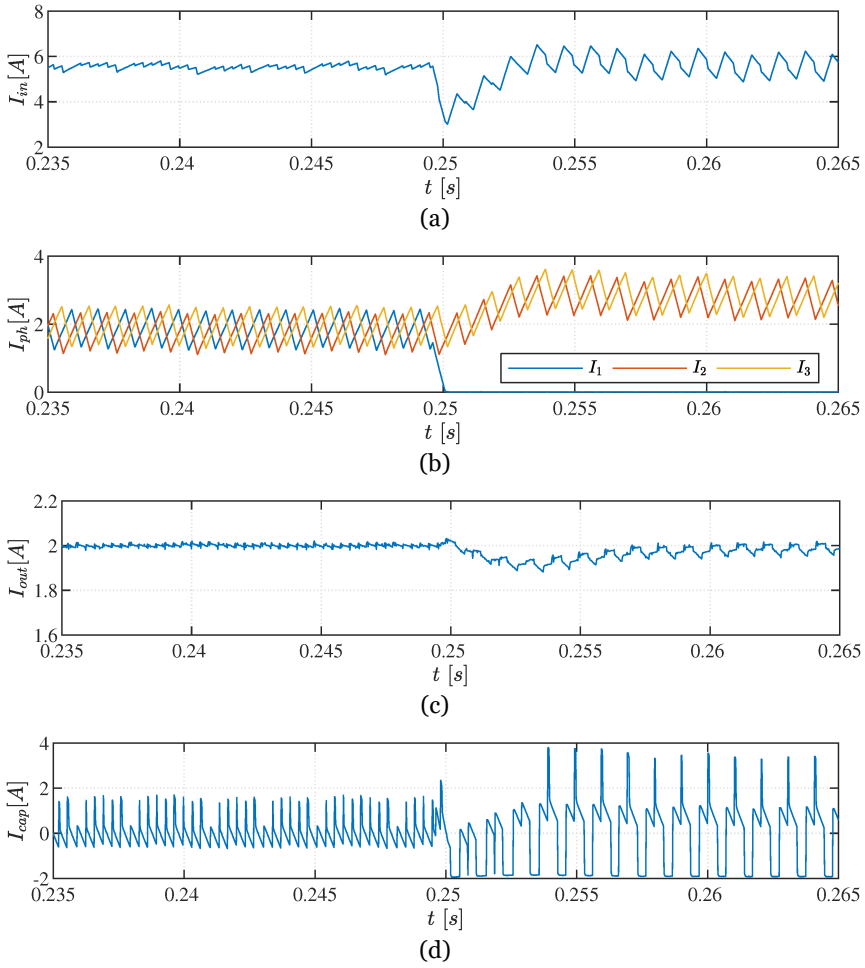


Fig. 4.7 Evolution, in time, of the most relevant converter variables: (a) Converter input current I_{in}; (b) Phase currents $I_{1...3}$; (c) Converter output current I_{out}; and (d) Output capacitor current I_{cap}. An OC fault occurs at t = 0.2496 s, in IGBT Q_1.

As expected, all the variables show evolution patterns similar to the ones shown in simulation, for the corresponding scenario (Fig. 4.4), thus confirming the consistency of the results. Despite such consistency, it is possible to observe some expected low amplitude, high frequency white noise on the converter output current I_{out} – refer to Fig. 4.7 (c).

Fig. 4.8 depicts the waveforms of the most relevant converter variables, showing their evolution in the pre-fault and post-fault periods, assessed at an output voltage V_{out} of 60 V and switching frequency f_{sw} of 3 kHz. The equivalent simulation results are provided in Fig. 4.5.

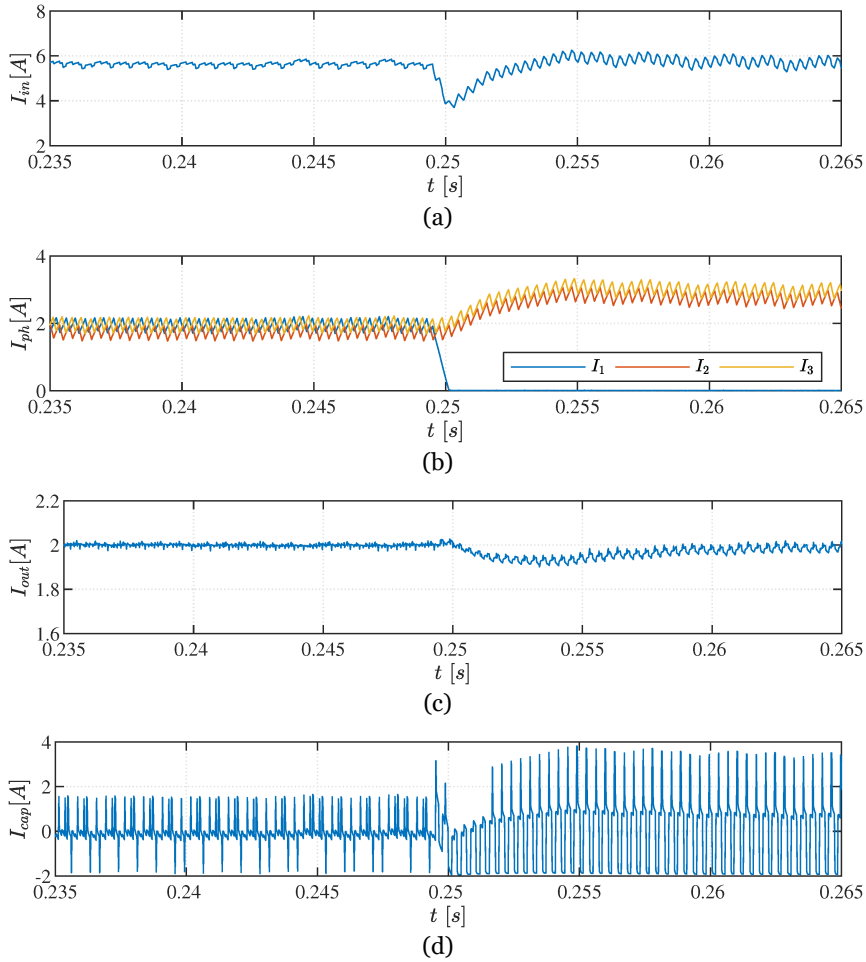


Fig. 4.8 Evolution, in time, of the most relevant converter variables: (a) Converter input current I_{in}; (b) Phase currents $I_{1...3}$; (c) Converter output current I_{out}; and (d) Output capacitor current I_{cap}. An OC fault occurs at t = 0.2496 s, in IGBT Q_1.

Once again, all the variables show evolution patterns similar to the ones shown in simulation, for the corresponding scenario (Fig. 4.5), thus confirming the consistency of the results.

4.2. LED lighting

4.2.1. Fault-tolerant SIMO converter

The following analysis focus on the evaluation of the 2-channel configuration of the fault-tolerant SIMO converter, depicted in Fig. 3.5.

To simplify the theoretical analysis of the converter operation, a few assumptions/simplifications are taken:

1) The dimming function of the LED driver is neglected at this stage. Consequently, the average current in each output of the LED driver is equal to the instantaneous string current:

$$\bar{I}_{1,2} = I_{\max_{1,2}} = I_{1,2} \tag{4.7}$$

2) The converter operates in CCM, regardless of the converter condition (healthy or faulty). Such assumption is taken provided that the studied converter topology is designed to drive multiple high-power LED strings. For those circumstances, CCM provides relevant advantages, in terms of current ripple and conversion efficiency, over the converter operation in DCM.
3) All strings employ identical LED devices, sharing the same parameters of the equivalent circuit.

One more important remark to consider has to do with the fact that the selected converter control strategy adopts a time-sharing scheme. Therefore, the analysis of the LED driver operation in healthy and faulty conditions should evaluate, individually, the timeslots assigned to each driver channel. In practice, this statement implies that variables like the semiconductors on-time or duty ratio are computed independently for each timeslot.

4.2.1.1. Operation principles under healthy condition

Given the characteristics of the selected LED driver and the nature of LED lighting loads, the analysis of the evolution over time of the inductor current provides important clues about the current supplied to each LED string, thus allowing to evaluate any potential degradation on the amount and quality of light delivered by the lighting system, as a whole.

Fig. 4.9 provides a general view on the switching pattern applied to the switches with current control functions, and the resulting inductor current, considering a scenario of healthy converter operation.

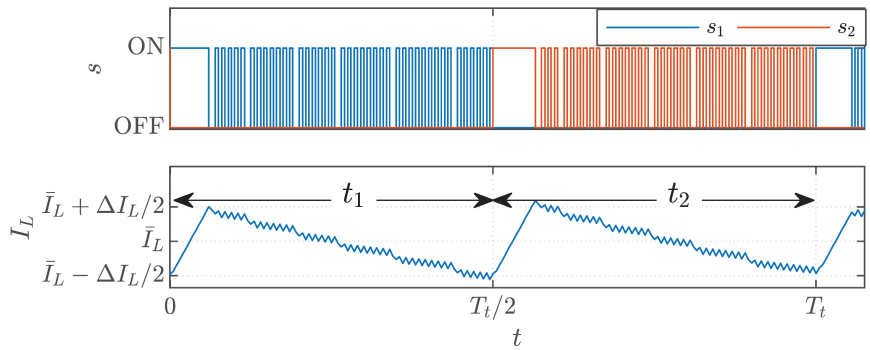


Fig. 4.9 Gating signals s_1 and s_2, applied to switches S_1 and S_2, respectively, and corresponding inductor current I_L. The converter operates in healthy condition.

As depicted in Fig. 4.9, the waveform of current I_L oscillates $\pm\Delta I_L / 2$ around the average value $\bar{I}_L$. Identical evolution is witnessed in all timeslots, provided that the inductor charging and discharging operation is uniform and evenly distributed over time. Each timeslot has a duration of $T_t / 2$, for the 2-channel LED driver under analysis.

In a classical single-output buck converter, the average inductor current equals the average output current. For the 2-channel SIMO LED driver considered in this study, the average inductor current equals the sum of the average currents measured in each output of the LED driver:

$$\bar{I}_L = \sum I_n = I_1 + I_2. \tag{4.8}$$

For the conditions considered in this study (a multi-output LED driver, operated in CCM, adopting a time-sharing modulation scheme), the following relation between the output and input voltages holds:

$$V_{C_n} = V_{in} d(t_n), n = 1,2 \tag{4.9}$$

where V_{Cn} denotes the output voltage at channel n, measured at the terminals of capacitor C_n, V_{in} refers to the input voltage, and $d(t_n)$ denotes the duty ratio observed for the timeslot t_n. As the duty ratio must be evaluated, independently, for each timeslot, the following formula should be considered for the 2-channel LED driver:

$$d(t_n) = \frac{t_{on}}{T_t}, n = 1,2 \tag{4.10}$$

where T_t denotes the period of the time-sharing carrier signal and t_{on} refers to the on-time measured during the period T_t.

Taking into account the circuit of the LED driver and the model of the LED device, it is possible to express the voltage of each output as the sum of the voltage drops in the LEDs themselves and in the current sensing resistor:

$$\begin{gathered} V_{C_n} = xV_{LED_n} + V_{R_{S\_n}} \Leftrightarrow \\ \Leftrightarrow V_{C_n} = x\left(R_{LED_n}\left(\bar{I}_L - I_n\right) + V_E\right) + V_{R_{S\_n}}, n = 1,2 \end{gathered} \tag{4.11}$$

where x specifies the number of LEDs of the string, V_{LEDn} denotes the voltage at the terminals of each LED device, V_{RS_n} refers to the voltage drop across the current sensing resistor, R_{LEDn} denotes the equivalent resistance of each LED device, and V_E refers to the forward voltage drop of each LED.

Still, in its present form, (4.11) does not provide useful information about $\bar{I}_L$. Resorting to (4.8) and (4.9) to reshape (4.11), the following expression is obtained:

$$\bar{I}_L = \frac{V_{in}\left(d(t_1)+d(t_2)\right)-2xV_E}{xR_{LED}+R_S}. \tag{4.12}$$

From (4.12), it is shown that $\bar{I}_L$ depends on well-defined, constant parameters of the system, like the LED devices properties or the converter input voltage. Therefore, the determination of current $\bar{I}_L$ is solely dependent on the sum of the duty ratios observed along the two timeslots (t_1 and t_2) that comprise a complete period of the time-sharing carrier.

Provided that all strings employ identical LED devices, the duty ratio can be assumed equal in all timeslots, for healthy converter operation:

$$d(t_1) = d(t_2) = d. \tag{4.13}$$

Hence, (4.12) can be further simplified:

$$\bar{I}_L = 2\frac{V_{in}d - xV_E}{xR_{LED}+R_S}. \tag{4.14}$$

Based on (4.14), it is possible to determine the individual string currents, as the average inductor current $\bar{I}_L$ is evenly distributed among the two outputs of the LED driver:

$$I_1 = I_2 = \frac{V_{in}d - xV_E}{xR_{LED}+R_S}. \tag{4.15}$$

4.2.1.2. Operation principles under OC fault condition

In the event of an OC fault in any of the switches with current control functions (S_1 and S_2), the current control function is lost during the timeslots assigned to the faulty channel. As a consequence, the inductor current decreases linearly during those timeslots. Since there is an uncontrolled current flow in the inductor during those timeslots, the current flowing through the faulty channel will potentially reduce, as a consequence of the switch fault.

The analysis presented hereafter considers a scenario of OC fault in switch S_2 of the 2-channel LED driver adopted in this study. One of the most noticeable consequences of the OC fault is the loss of the switching action during the timeslots assigned to the faulty switch. Given the fault condition, it is possible to assume that the switching duty ratio observed over the timeslot t_2 is null:

$$d(t_2)' = 0. \tag{4.16}$$

On the other hand, the maximum switching duty ratio observed for the timeslot assigned to the healthy switch (t_1) gets limited to 0.5, in the case of the 2-channel driver under evaluation:

$$d\left(t_{1_{max}}\right)' = 0.5 \tag{4.17}$$

where $d(t_{1_{max}})'$ denotes the maximum duty ratio observed for timeslot t_1, during the post-fault period.

In the event of an OC fault in switch S_2, the average inductor current observed in faulty state $\bar{I}_L'$ depends on the switching duty ratio observed in the pre-fault period. Two conditions can be observed: 1) the sum of the pre-fault duty ratios $d(t_1)$ and $d(t_2)$ does not reach 0.5; and 2) the sum of the pre-fault duty ratios $d(t_1)$ and $d(t_2)$ surpasses 0.5. According to those two scenarios, current $\bar{I}_L'$ is computed as follows:

$$\bar{I}_L' = \begin{cases} 2\dfrac{V_{in}d(t_1)' - xV_E}{xR_{LED}+R_S} = \bar{I}_L, \text{ if } d(t_1)+d(t_2)<0.5 \\ \dfrac{V_{in}d(t_1)' - xV_E}{xR_{LED}+R_S} < \bar{I}_L, \text{ if } d(t_1)+d(t_2)\geq 0.5 \end{cases}. \tag{4.18}$$

Based on (4.18), it is observed that current $\bar{I}_L$ is kept unchanged for the post-fault period, as long as the sum of the switching duty ratios observed during the pre-fault period does not reach 0.5. For this condition, the current is equally shared among both LED strings:

$$I_1' = I_2' = \frac{V_{in}d(t_1)' - xV_E}{xR_{LED}+R_S}. \tag{4.19}$$

Fig. 4.10 provides a general view on the switching pattern applied to the switches with current control functions, and the resulting inductor current I_L, considering a scenario of faulty converter operation, in case that condition $d(t_1) + d(t_2) < 0.5$ holds.

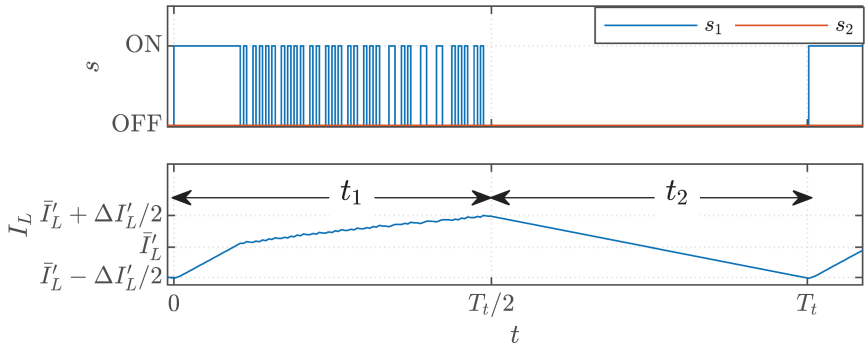


Fig. 4.10 Gating signals s_1 and s_2, applied to switches S_1 and S_2, respectively, and corresponding inductor current I_L. An OC fault impairs the operation of switch S_2.

As depicted in Fig. 4.10, the waveform of current I_L oscillates $\pm\Delta I_L'/2$ around the post-fault average current $\bar{I}_L'$, which remains equal to the average current observed in the pre-fault period $\bar{I}_L$, despite the OC fault in switch S_2. On the other hand, the ripple of the inductor current increases for the post-fault period $(\Delta I_L' > \Delta I_L)$. Consecutive inductor charging and discharging cycles occur for the timeslots assigned to the healthy channel,

while a single discharging cycle takes place during each one of the timeslots assigned to the faulty channel.

On the other hand, and also according to (4.18), it is observed that the average inductor current suffers a depreciation for the post-fault period, in case that condition $d(t_1) + d(t_2) \geq 0.5$ holds. Such operation condition implies a degradation on the current supplied to the string of the faulty channel (I_2') and, eventually, on the current supplied to string 1 (I_1'). Accordingly, the individual string currents are computed as follows:

$$I_1' = \frac{V_{in} d(t_1)' - 2xV_E}{2(xR_{LED} + R_S)}, \tag{4.20}$$

$$I_2' = \frac{V_{in}(1 - d(t_1)') - 2xV_E}{2(xR_{LED} + R_S)}. \tag{4.21}$$

Fig. 4.11 depicts the switching pattern applied to the switches with current control functions, and the resulting inductor current I_L, considering a scenario of faulty converter operation, in case that duty ratio $d(t_1) + d(t_2)$ surpasses 0.5.

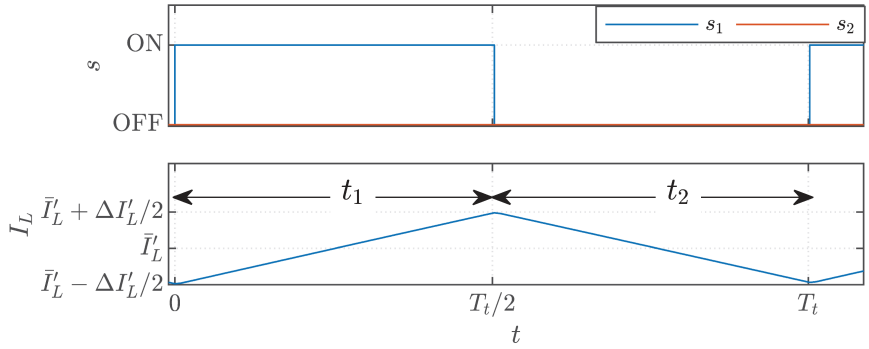


Fig. 4.11 Gating signals s_1 and s_2, applied to switches S_1 and S_2, respectively, and corresponding inductor current I_L. An OC fault impairs the operation of switch S_2.

For the conditions depicted in Fig. 4.11, the current controller is not able to track the reference current for the timeslot t_2. As a result, the post-fault average current $\bar{I}_L$' decreases, in comparison to the average current observed in the pre-fault period $\bar{I}_L$.

4.2.1.3. Simulation results

To evaluate the operation of the fault-tolerant SIMO LED driver under both healthy and OC fault condition, a simulation model was developed resorting to the software *Simulink*™. Further details regarding the simulation model, its architecture and the parameters considered for the evaluation are provided in Appendix A.2.

In the simulated scenarios, both the 2-channel and 4-channel architectures of the LED lighting system are tested for multiple dimming ratios and current references.

Fig. 4.12 depicts the waveforms of the string currents, obtained for the 2-channel configuration of the lighting system. Both channels apply a dimming ratio of 0.2 and a current reference equal to 0.5 A.

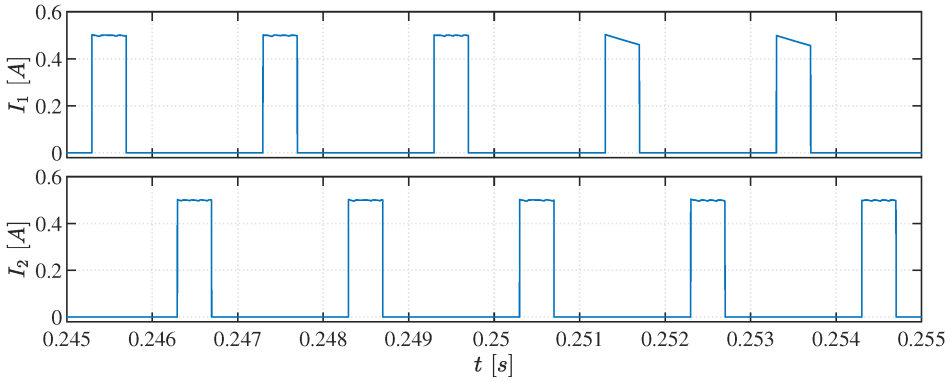


Fig. 4.12 LED string instantaneous currents in a 2-channel driver. The dimming ratio d_{dim} is 0.2 in all strings, while the current reference I_{ref} is 0.5 A in all strings. An OC fault occurs in switch S_1, at t = 0.25 s.

As a consequence of the fault, taking place at t = 0.25 s, only the healthy channel is capable of performing the current control function. While the current at String 2 is kept constant at 0.5 A for the on-time period, the current in String 1 suffers a minor depreciation during the corresponding on-time period.

It is well known that the luminous flux delivered by a LED string has a direct correlation with the average current flowing through that string. Since the current flowing through the string associated to a faulty channel $\bar{I}_n$ is not constant during the on-time period, $\bar{I}_n$ should be computed as the integral of the current over the dimming period T_{dim}:

$$\bar{I}_n = \frac{1}{T_{\text{dim}}} \int_{0}^{T_{\text{dim}}} I_n \, dt. \tag{4.22}$$

$\bar{I}_n$ denotes the average current in the string associated to the faulty channel, T_{dim} (T_{dim} = 1/f_{dim}) denotes the dimming period, and I_n refers to the instantaneous string current.

Based on the information of the average current, it is possible to compute the relative depreciation of the string current, described using (4.23):

$$\Delta I_n = \frac{\bar{I}_n(\text{pre-fault}) - \bar{I}_n(\text{post-fault})}{\bar{I}_n(\text{pre-fault})} \times 100. \tag{4.23}$$

Fig. 4.13 depicts the average current measured at both LED strings, for the conditions defined in Fig. 4.12.

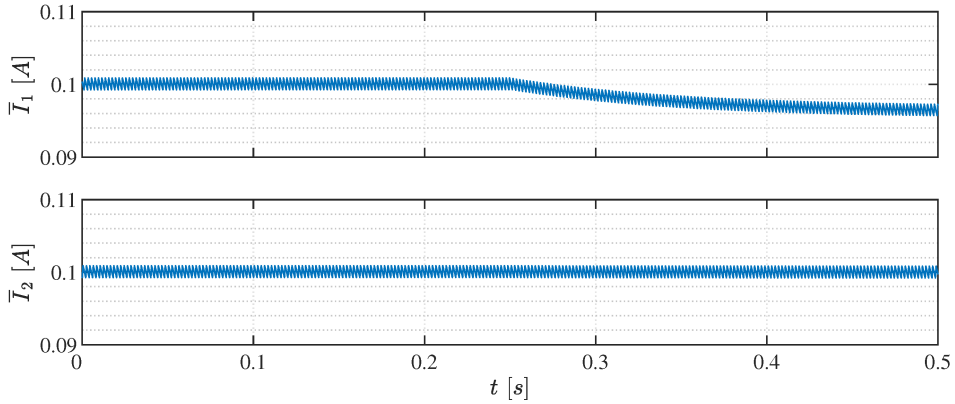


Fig. 4.13 LED string average currents in a 2-channel driver. The dimming ratio d_{dim} is 0.2 in all strings, while the current reference I_{ref} is 0.5 A in all strings. An OC fault occurs at switch S_1, at t = 0.25 s.

Following the OC fault at switch S_1, occurring at t = 0.25 s, a depreciation of 3.3 % of the average current flowing through String 1 is verified. It is small yet important depreciation on the average current, with impact on the expected luminous flux. The degree of depreciation on the average current is partially explained by the low dimming ratio. String 2 holds the pre-fault average current level and, consequently, maintains the same luminous flux.

To evaluate the impact of variations on the dimming ratio and current reference, a second scenario was established and evaluated in the 2-channel configuration. Fig. 4.14 depicts the waveforms of the instantaneous string currents, before and after an OC fault in switch S_2.

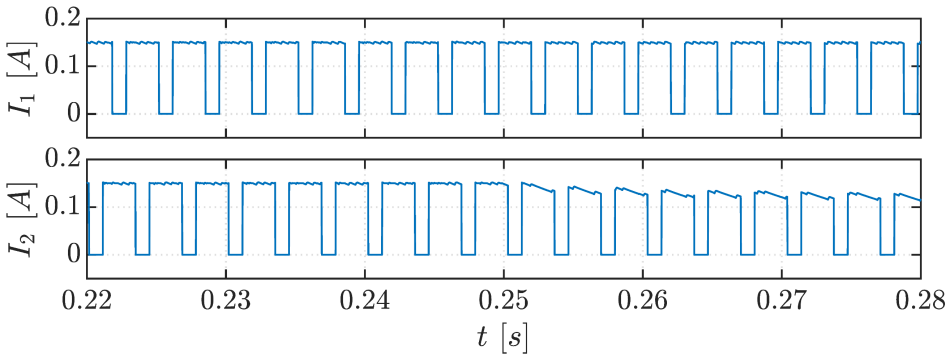


Fig. 4.14 LED string instantaneous currents in a 2-channel driver. The dimming ratio d_{dim} is 0.7 in all strings, while the current reference I_{ref} is 0.15 A. An OC fault occurs in switch S_2, at t = 0.25 s.

The results provided in Fig. 4.14 show that the OC fault at switch S_2 does not introduce perturbations on the waveform of current I_1. Accurate current control capability is lost at String 2, resulting in a relevant depreciation of current I_2.

Fig. 4.15 shows the evolution, in the time domain, of the average string currents $\bar{I}_1$ and $\bar{I}_2$, for the operation conditions presented in Fig. 4.14.

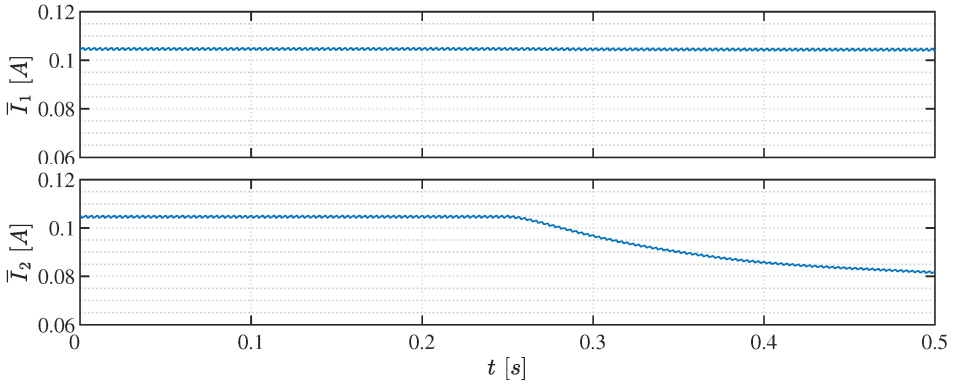


Fig. 4.15 LED string average currents in a 2-channel driver. The dimming ratio d_{dim} is 0.7 in all strings, while the current reference I_{ref} is 0.15 A. An OC fault occurs in switch S_2, at t = 0.25 s.

As expected, the OC fault at switch S_2 does not perturb the average string current $\bar{I}_1$. With regard to the average string current $\bar{I}_2$, the depreciation of current $\bar{I}_2$ exceeds 20 % of the pre-fault average current. For this scenario, the more prominent decay on current $\bar{I}_2$ can be explained by the adopted dimming ratio.

Quite often, the operation of power converters is impaired by multiple faults, which may take place successively. Hence, a scenario where multiple switches fail simultaneously cannot be obviated. As a consequence of those faults, the average current measured in the strings connected to the faulty channels decreases. Naturally, the luminous flux of the affected LED strings decreases as well. For illustrative purposes, let us consider the 4-channel configuration of the fault-tolerant SIMO LED driver and suppose that switches S_1, S_2, and S_3 fail. As a result of that condition, the luminous flux slightly deteriorates in String 1, String 2, and String 3. On the other hand, String 4 does not suffer any deterioration of the luminous flux, as the average current remains unchanged on that string.

Fig. 4.16 depicts the waveforms of the LED strings' currents, assessed for the scenario of multiple failures, where three simultaneous OC faults impair switches S_1, S_2, and S_3.

As a consequence of the faults, only String 4 sustains the current, during the on-time period, at the reference value of 0.5 A. The current decreases in all other LED strings during the corresponding on-time periods.

As demonstrated in Fig. 4.17, the average current drops in the strings that suffer the effects of OC faults. In this case, there is a drop of up to 28.6 % in the average current of the three LED strings connected to faulty channels. The decay is uniform and evenly distributed over the strings connected to faulty channels.

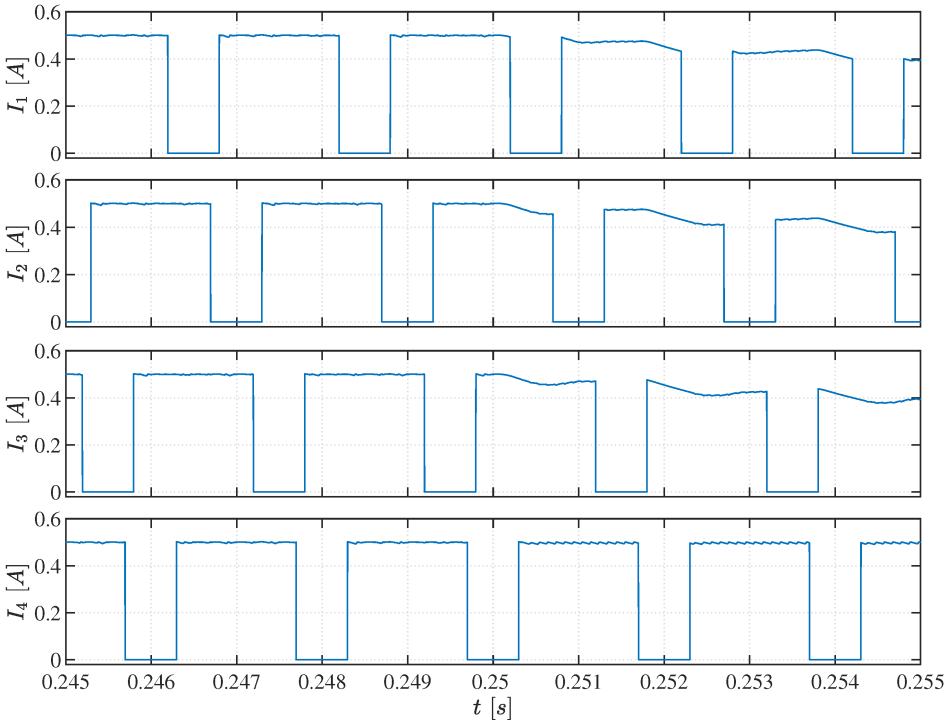


Fig. 4.16 LED string instantaneous currents in a 4-channel driver. The dimming ratio d_{dim} is 0.7 in all strings, while the current reference I_{ref} is 0.5 A in all strings. OC faults occur at switches S_1, S_2, and S_3 at t = 0.25 s.

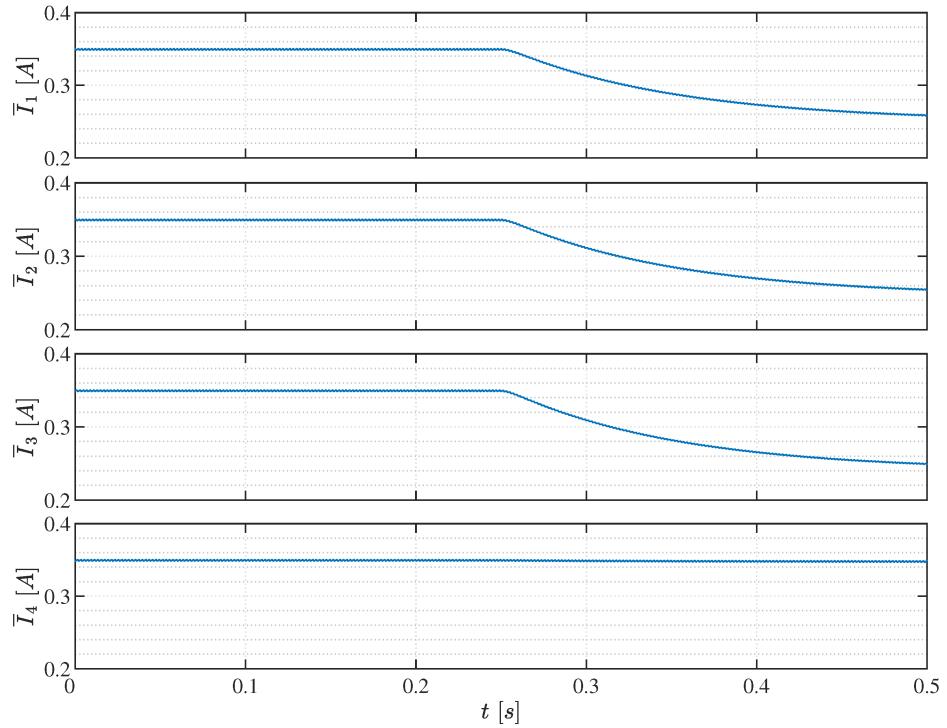


Fig. 4.17 LED string average currents in a 4-channel driver. The dimming ratio d_{dim} is 0.7, while the current reference I_{ref} is 0.5 A in all strings. OC faults occur at switches S_1, S_2, and S_3 at t = 0.25 s.

The major and most noticeable effect of OC faults in the switches of the converter is the depreciation of the LEDs forward current which, in turn, translates into a depreciation

of the luminous flux of the LEDs. Given the linear relation between the forward current and the luminous flux, it is possible to estimate the degree of depreciation of the luminous flux of a LED, resorting to information of the LED datasheet. That degree of depreciation in the luminous flux of a LED light strongly depends on its technical features. Taking the LED described in [47] as example, a depreciation of 12.5 % in the forward current results in a decrement of the luminous flux by nearly 20 %. Meanwhile, a depreciation of 6.7 % in the forward current of the LED described in [48] results in identical decrement of the luminous flux (20 %).

The severity of the deterioration in the luminous flux mainly depends on the number of channels affected by OC faults. Fig. 4.18 establishes a relation between the relative depreciation of the average current ΔI_n, observed in each LED string, and the number of OC faults in the LED driver, considering distinctive dimming ratios and levels of current reference.

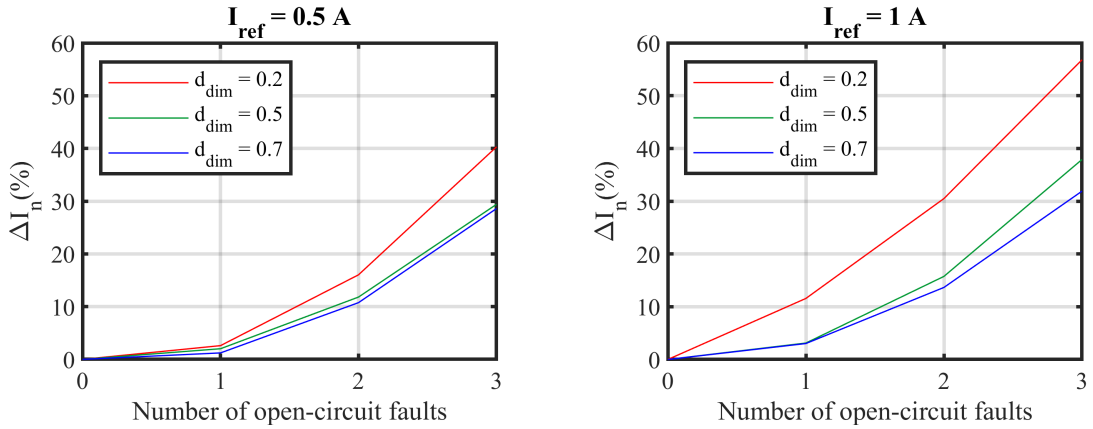


Fig. 4.18 Relative depreciation of the average string current as a function of the number of open-circuited switches among the group of switches S_1 ... S_n, considering distinctive dimming ratios. The results, assessed for a 4-string LED driver, are provided for two levels of current reference: (a) $I_{ref} = 0.5\ A$; (b) $I_{ref} = 1\ A$.

Note that the results shown in Fig. 4.18 are valid for the simulated 4-string LED driver and the selected LED driver parameters. As shown in Fig. 4.18, the depreciation of the current in the faulty LED strings has a strong dependence on the number of faulty channels. As mentioned before, it is feasible to continuously supply all LED strings, even in the worst-case scenarios, i.e., the scenarios with fewer functional current control switches.

As noted in Fig. 4.18, a single OC fault does not have a significant impact on the light emitted by the group of LED strings. Only one of the strings suffers a minor depreciation of the average current, which does not surpass 5 % of the pre-fault average current. As the number of faulty channels increases, the depreciation of the current assumes an exponential trend.

An important remark to take from the results of Fig. 4.18 is the fact that the adoption of smaller levels of the current reference I_{ref} has the potential to curtail the depreciation of the current in the faulty LED strings.

4.2.1.4. Experimental results

Experimental tests were developed to confirm the analytical model and the simulation results presented in the previous section. The parameters of the converter components are identical to those used in simulation. Further information regarding the experimental setup and the parameters of the system are available in Appendix B.2.

Fig. 4.19 depicts the waveforms of the currents flowing through each LED string, considering both healthy and OC fault conditions. An OC fault is introduced in switch S_2, at $t = 0.25\ s$. The scenario presented herein adopts conditions equivalent to the ones considered for the simulation results presented in Fig. 4.14.

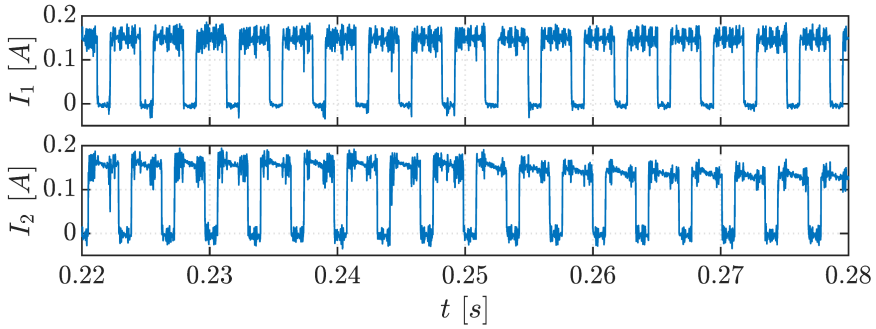


Fig. 4.19 LED string instantaneous currents (I_1 and I_2) in a 2-channel driver. The dimming ratio d_{dim} is 0.7 in both LED strings, while the current reference I_{ref} is 0.15 A. An OC fault occurs in switch S_2, at $t = 0.25\ s$.

Apart the slightly higher presence of high-frequency noise, not noticed on the simulation results, there is a good agreement between the experimental results obtained for the instantaneous string currents I_1 and I_2, and the corresponding simulation results, provided at Fig. 4.14, thus confirming the accuracy and usefulness of the simulation model. The random noise observed in the results can be assigned to a couple of potential sources, being the parasitic inductances and capacitances of the circuit the most likely ones.

Fig. 4.20 shows the evolution, in the time domain, of the average string currents $\bar{I}_1$ and $\bar{I}_2$, for the operating conditions depicted in Fig. 4.19.

As expected, the results of Fig. 4.20 show a significant degree of correspondence between simulation and experimental tests. Under healthy condition, currents $\bar{I}_1$ and $\bar{I}_2$ successfully track the desired current reference. On the other hand, current $\bar{I}_2$ suffers a relevant depreciation as a consequence of the OC fault at switch S_2, decreasing from the 0.104 A measured for healthy condition, to the 0.089 A measured after the OC fault at switch S_2.

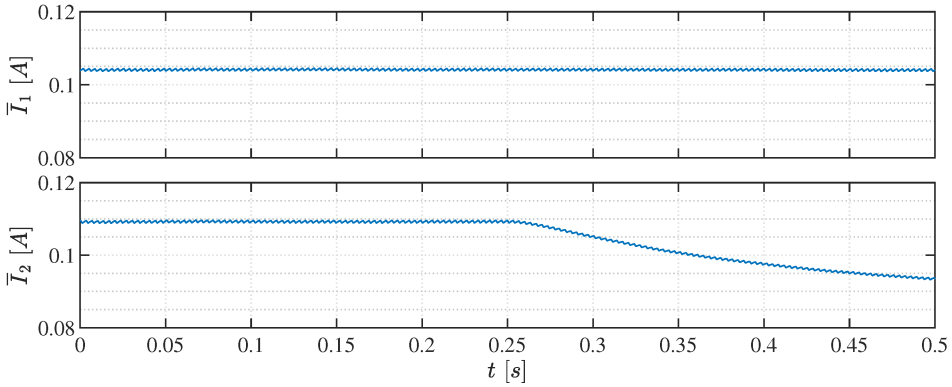


Fig. 4.20 LED string average currents ($\bar{I}_1$ and $\bar{I}_2$) in a 2-channel driver. The dimming ratio d_{dim} is 0.7 in both LED strings, while the current reference I_{ref} is 0.15 A. An OC fault occurs in switch S_2, at $t = 0.25\ s$.

Chapter 5

Fault diagnosis in DC–DC converters

The ever-increasing adoption of DC–DC converters has been witnessed in an extended range of applications, such as renewable energies, energy storage systems, consumer electronics, general appliances, or LED lighting, to name a few. Along with such evolution, there is an increasing need to obtain more efficient, cheap, and reliable DC–DC converters.

The research efforts made towards the improvement of the availability and reliability of DC–DC converters are still quite narrow and scattered. Moreover, DC–DC converters take the shape of an endless number of topologies, with different functions and operation principles, thus complicating the task of improving the availability and reliability of all forms of DC–DC converters. As any other energy conversion system based on power electronics, DC–DC converters are continuously subjected to a plethora of stress factors, such as electrical, thermal and physical stress. The conjunction of all these stress factors lead to potential early degradation of the converter components, thus limiting the overall useful lifetime of DC–DC converters. Within DC–DC converters, power semiconductors and, particularly, power switches – IGBTs, metal oxide semiconductor field effect transistors (MOSFETs) – constitute the group of susceptible components showing higher failure rates. Indeed, this fact explains why recent reliability studies addressing DC–DC converters concentrate efforts on finding advanced solutions for the diagnostic and prognostic of faults in power switches.

This chapter focuses attentions on the diagnosis of failures on the power semiconductors of DC–DC converters. The chapter begins with a thorough analysis of the most relevant advancements achieved so far concerning the diagnostic of power semiconductor failures. Special emphasis is given to the diagnostic techniques intended for detection and identification of OC and short-circuit (SC) faults. Afterwards, the novel contributions introduced in this thesis are described and detailed. To demonstrate the effectiveness of those contributions, simulation and experimental data is compiled and analysed in detail.

5.1. State-of-the-art fault diagnostic strategies

Most fault diagnostic techniques currently available in the literature, suitable for DC–DC converters, aim the diagnostic of OC and SC faults in the converter power switches [49], [50]. Such concentration of efforts is explained by the fact that semiconductor faults prevail among the most common and critical failure modes of any DC–DC converter. To diagnose switch faults, the algorithms commonly rely on the analysis of converter variables, such as the input current or the DC-bus capacitor voltage. These variables are commonly referred to as diagnostic variables.

OC faults often derive from failures in the gate drivers, soldering break or wire lifting [9]. In a wide group of DC–DC converter topologies, OC faults do not pose a prominent threat to the converter core components that remain healthy: the energy transfer to the load is commonly sustained, under degraded conditions (more ripple, lower conversion efficiency, etc.). Still, if such faults remain undetected for long periods, further damages might be incurred in the converter and, in extreme cases, lead to its total standstill. Therefore, the detection and identification of such failures is critical, as it prevents the extension of more severe damages inside the power converter.

Concurrently, SC faults in the converter switches are severe fault events that must be detected and isolated within a few microseconds. Many diagnostic algorithms simply dismiss any capabilities for diagnostic of SC faults. Many arguments are evoked for not considering SC faults in the diagnostic of switch faults:

1) Typically, SC faults are isolated from the rest of the converter circuit resorting to hardware protection devices, namely fuses, and usually result in a very limited or, sometimes, impossible operation of the converter;
2) SC faults are commonly followed by OC faults, as a result of isolation actions carried out via hardware;
3) SC faults require a fast response of the control structure, in order to isolate the fault and avoid extended damages in the converter or any other equipment connected to it. Generally, software protections do not provide the ultra-fast response required to overcome the effects of SC faults.

The diagnostic of power switches faults in DC–DC converters is usually made online and takes place in two distinctive stages: fault detection and fault identification. At the fault detection stage, a fault alarm is triggered; the faulty component and corresponding fault mode remain unknown. During the fault identification stage, the fault mode and the component that has given rise to the fault alarm are identified. Certain fault diagnostic algorithms combine the detection and identification actions in a single stage, meaning that fault detection and identification actions are developed concurrently. Such practice mainly

depends on the capabilities of the adopted fault diagnostic algorithm and on the selected fault diagnostic variables.

There is not a unique, generally adopted, classification scheme of the fault diagnostic algorithms developed so far, aimed at semiconductor faults. Nevertheless, it is possible to establish a classification scheme, by taking into account the information required to implement each algorithm. Fig. 5.1 shows a simplified classification scheme of the state-of-the-art fault diagnostic algorithms.

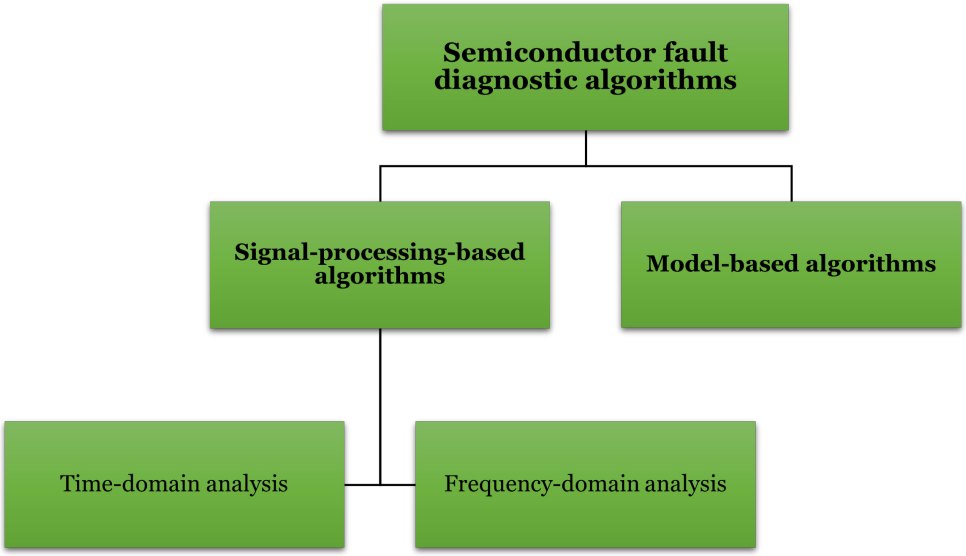


Fig. 5.1 Classification of the semiconductor fault diagnostic algorithms aimed at DC–DC converters.

Most fault diagnostic algorithms aimed at DC–DC converters obtain fault signatures based on certain variables of the converter, sensed in real time. For the purpose of this thesis, such algorithms are categorised as 'signal-processing-based algorithms', since the diagnostic action is solely supported by the analysis of fault signatures, extracted from converter variables whose evolution is perturbed by faults in the converter switches.

More recently, alternative diagnostic algorithms, with improved robustness against false fault alarms, have been introduced. These algorithms are referred to as 'model-based algorithms' since the diagnostic action is supported by a pre-established converter model. Next sub-sections provide deeper insight about each one of the aforementioned categories.

5.1.1. Signal-processing-based fault diagnostic algorithms

Fault diagnostic algorithms based on signal processing techniques represent the largest share of algorithms available in the literature, aimed at diagnosing power switches' faults in DC–DC converters. These algorithms identify certain fault signatures resorting to an analysis of carefully selected converter variables, commonly used for control purposes, as for instance DC-bus current or capacitors voltage. As illustrated in Fig. 5.2, either the converter input, output or other internal variables are sensed and subjected to signal

processing techniques. The adopted signal processing techniques for diagnostic purposes strongly depend on the selected diagnostic variables.

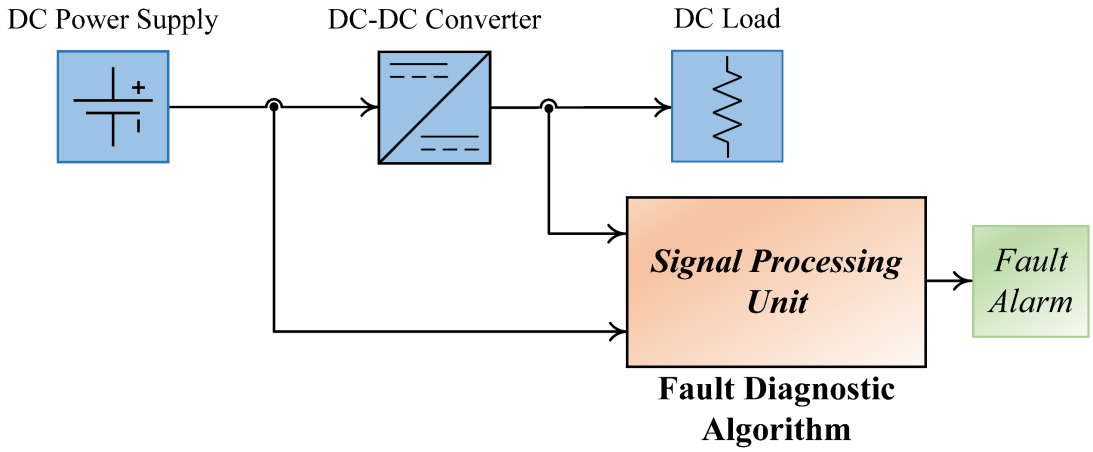


Fig. 5.2 Principles of implementation of a signal-processing-based fault diagnostic algorithm aimed at DC–DC converters.

The success that these fault diagnostic algorithms achieved so far is mainly justified by the simplicity, the reduced computational effort required to implement the algorithms and by the adoption of black-box approaches. Furthermore, there is the possibility to implement the same algorithm in several DC–DC converter topologies, depending on the capabilities of the fault diagnostic algorithm. Therefore, a quite straightforward analysis is adopted, especially when there is no previous knowledge about the converter parameters. The adoption of a black-box approach, typical of signal-processing-based algorithms, provides the interesting attribute of obviating the need for detailed knowledge of the DC–DC converter parameters. Unfortunately, the action of signal-processing-based diagnostic algorithms might not be totally effective, since false fault alarms might be triggered when the converter is required to operate under a highly dynamic operation pattern, with significant oscillations in the load levels, switching frequencies or conduction modes, leading to inaccurate diagnostic results.

As shown in Fig. 5.1, it is possible to establish a thinner classification of signal-processing-based diagnostic algorithms, by taking into account whether the diagnostic variables are evaluated in the time or frequency domains.

5.1.1.1. Time-domain signal-processing-based algorithms

As the denomination itself suggests, these algorithms implement an analysis, in the time domain, of the variables selected for diagnostic purposes. Such analysis may rely on a variety of methodologies, including magnitude analysis, trend analysis, limit evaluation, mean values assessment, statistical moments, etc.

Certain fault diagnostic algorithms based on time-domain analyses are designed to meet very specific requirements of some converter topologies or operation points. Therefore, the extrapolation of those algorithms to other converter topologies might be quite challenging or even impossible. In opposition, there are certain fault diagnostic algorithms based on time-domain analyses which, by virtue of their characteristics, provide a broad spectrum of action, allowing the proper extrapolation to several converter topologies. It is the case of algorithms based on converter variables present in most converter topologies, as for example the DC-bus current.

The wide range of fault diagnostic algorithms based on a time-domain analysis mainly differ on the selected diagnostic variables and on the methodologies used to extract relevant fault signatures. The requirement of thresholds for the decision-making process also depends on the architecture of the diagnostic algorithm. Often, gating signals complement the information provided by the diagnostic variables, allowing to easily locate the faulty component. While selecting diagnostic variables, researchers look forward to selecting diagnostic variables which fulfil the following requirements: 1) the requirement of additional sensors is obviated or, at least, reduced; and 2) several fault signatures are provided by that diagnostic variable, allowing to properly identify several fault modes or faulty components.

Older diagnostic tools applying time-domain analyses track anomalous deviations in the magnitude of converter variables using, for instance, statistical moments of the converter voltages and currents [51] or the input current peak to integral ratio [52] to diagnose OC faults in the target converter topologies. The implementation of these algorithms is quite simple and lies on simple analogue circuitry to detect switch faults. Even though the validation of the algorithms is solely confirmed for the cascaded converter [51] and full bridge (FB) zero-voltage switching (ZVS) DC–DC converter [52], the algorithms' nature enables the implementation of such diagnostic strategies in other converter topologies as well.

In simpler multilevel DC–DC converter assemblies, the DC-bus capacitors voltage balance, a condition which should be continuously met, is monitored to detect switch faults [53]. Despite the simplicity of the algorithm, the simple act of analysis of the DC-bus capacitors voltage does not provide conclusive information, in most situations, about the converter faulty component(s). The implementation of this algorithm on a three-level flying capacitor DC–DC converter comprises the comparison of the flying capacitor voltage with two distinctive thresholds. Based on the results of such comparison, it is possible to issue a fault alarm and, whenever feasible, to identify the faulty component.

When it comes to isolated DC–DC converter topologies, the transformer windings voltages are widely selected as diagnostic variables. The analysis of the windings' voltages

mean values has proven suitable to detect and identify switch faults in DC–DC converter topologies employing galvanic isolation [54]. The decision process of the algorithm requires the establishment of an empirical threshold. Identical fault diagnostic algorithm, equally based on the transformer primary-side voltage, compares the amplitude of this diagnostic variable to a predefined threshold, allowing to detect the presence of OC faults [55]. The reliable identification of the faulty component remains a challenge in [54], [55]. To overcome such difficulty, the voltage at the midpoint of each converter leg is sensed independently, as proposed in [56].

The inductor current slope is used as fault diagnostic variable in the diagnostic of power switches' faults in non-isolated single-ended converters. The measured inductor current slope sign is compared with the expected inductor current slope sign, ensuring fast and reliable diagnostic results [57]. Thereafter, a series of fault diagnostic algorithms, based on the same diagnostic variable and principles of operation, have introduced minor improvements in the effectiveness of the original fault diagnostic algorithm. One of those algorithms consists of two state machines, with a similar structure, operated in parallel to develop the fault diagnostic action [58]. The introduced modification allows to distinguish OC and SC faults, which was not available in the preliminary version of the algorithm. To slightly improve the diagnostic effectiveness, the non-ideal response of the converter is considered in the implementation of another derivation of the original algorithm. The fault diagnostic action compares the sign of the inductor current slope and a delayed version of the gating signal, intrinsic to the non-ideal converter [59]. Supported on the same diagnostic principles, simpler strategies, requiring less computational effort, were developed. The observation of the switch health condition, through the analysis of the inductor current slope sign during one switching period, is performed resorting to a single state machine [60], [61]. In a preliminary iteration [60], fault diagnostic is achieved, but there are no conclusive results about which fault mode impairs the switch (OC or SC fault), as shown in Fig. 5.3 (a). The transition between states, denoted as x_1 and x_2 in Fig. 5.3 (a), takes into account the information provided by gating signal q, depicted in Fig. 5.3 (b). Each transition is triggered by the edges of gating signal q, as depicted in Fig. 5.3 (b).

The problem of fault identification verified in the aforementioned algorithm [60] is overtaken by selecting different moments for the transition between machine states [61]. Fig. 5.4 (a) depicts a simplification of the flowchart followed by the state machine [61], while Fig. 5.4 (b) shows a timeframe which illustrates the moments in which the transitions between most meaningful states take place.

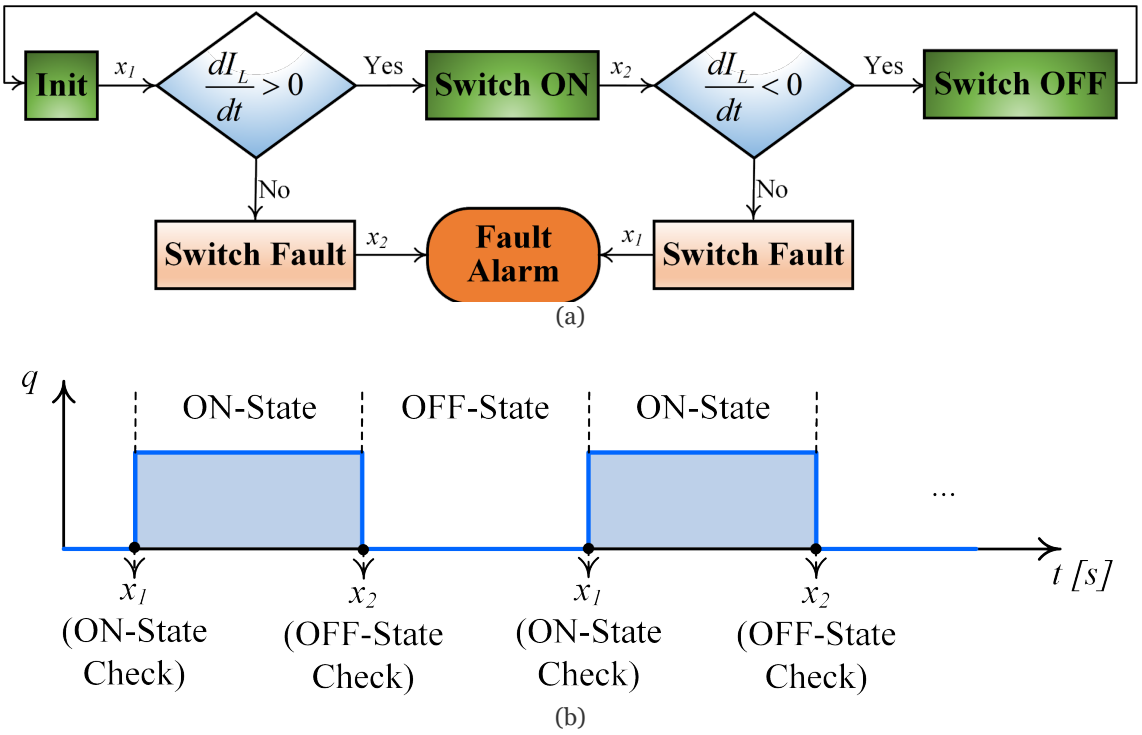


Fig. 5.3 (a) Flowchart of the state machine implementing a fault diagnostic algorithm based on the information of the inductor current slope [60]; (b) Gating signal q and instants used to control the transition between machine states [60].

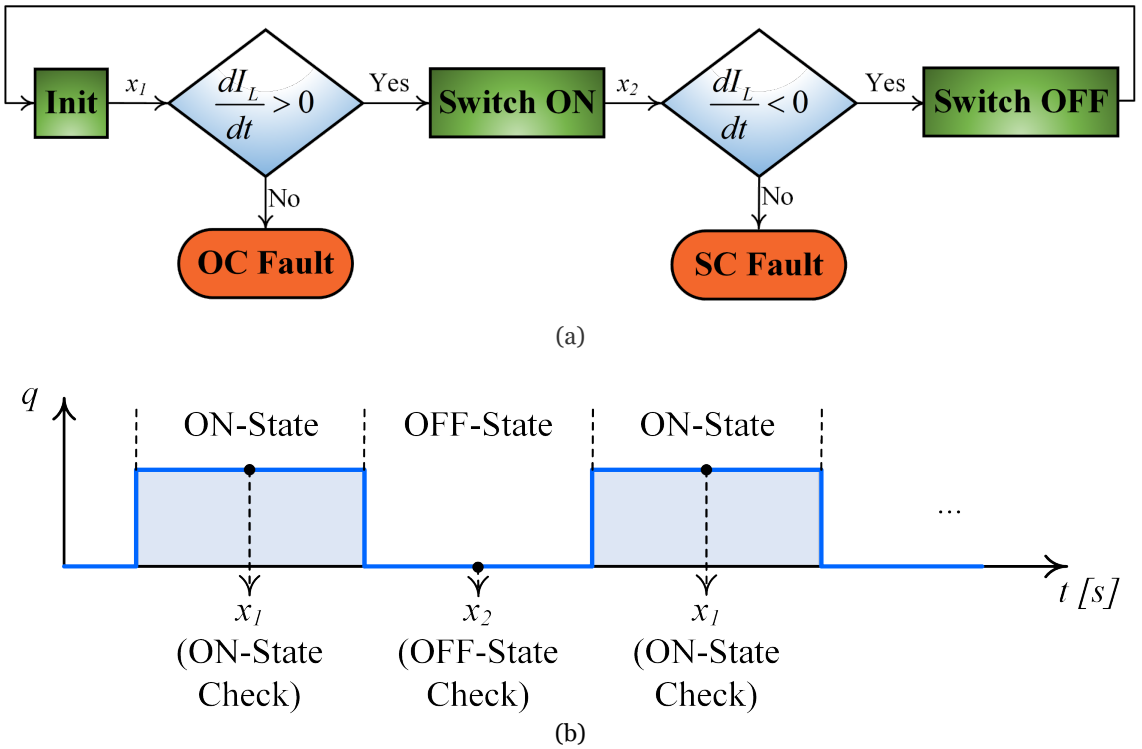


Fig. 5.4 (a) Flowchart of the state machine implementing an improved fault diagnostic algorithm, based on the sign of the inductor current slope [61]; (b) Gating signal q and instants used to control the transition between machine states [61].

To obtain optimised diagnostic results, certain fault diagnostic strategies are developed to meet the requirements of specific practical applications. In PV systems, the low frequency oscillations in the amplitude of PV variables (voltage, current and power) provide suitable information to detect switch faults [62]. A sequence of events, comprising the increment of the PV panel voltage, and the decrement of the PV panel current and power, reveal the occurrence of OC faults in the converter responsible for the maximum power point tracking (MPPT) control [62].

A significant group of fault diagnostic algorithms rely on analyses, in the time domain, of the inductor current amplitude. One of those algorithms, suitable for single-switch converters, selects strategic instants to sample the inductor current amplitude, aiming to establish logical relations between the sampled values. A comparison between the absolute values of the inductor current, sampled at three distinctive moments allows to identify faults in the converter switch [63].

Alternative approaches, based on the same diagnostic variable, take advantage of the gating signals information to sample the amplitude of the inductor current at the rising and falling edges. Variations of that fault diagnostic algorithm were successfully employed in a multi-input DC–DC converter [64], non-isolated bidirectional DC–DC converter [65], non-isolated unidirectional DC–DC converter [66], and in an interleaved DC–DC boost converter [67], [68]. As confirmed in Fig. 5.5, the logical relations between the current amplitude measured at the rising and falling edges of the gating signals are affected by OC faults in the converter switches. Indeed, it is a behaviour observed in all aforementioned converter topologies [64]–[68].

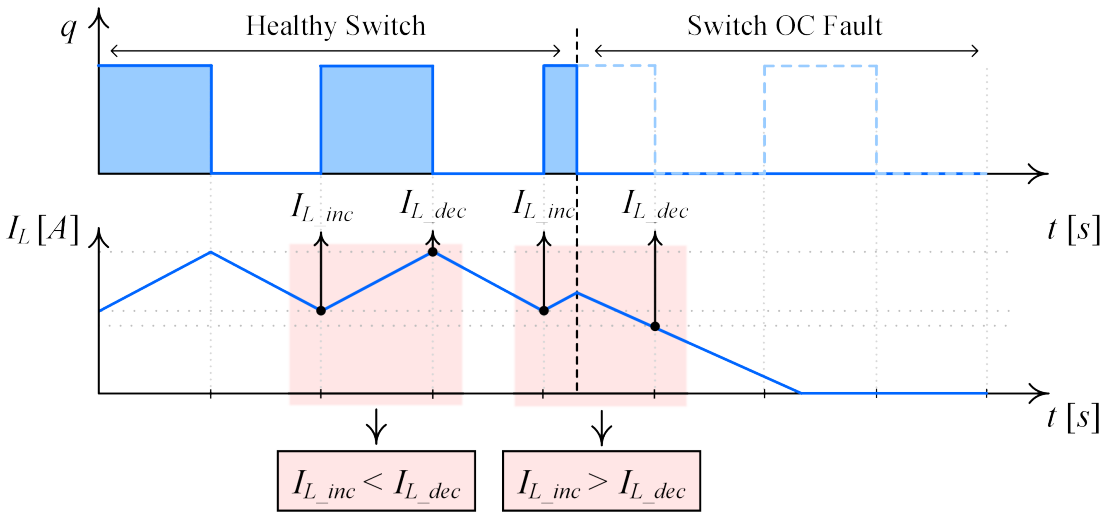


Fig. 5.5 Evolution of the inductor current in a non-isolated unidirectional buck converter, under healthy condition (first half of the switching pattern) and faulty condition (second half of the switching pattern).

Current amplitude also provides sufficient information for diagnostic of faults in parallel connected single-active-bridge (SAB) DC–DC converters [69]. The converter output current is sampled at pre-established moments, allowing to detect and even identify the module containing the faulty switch. The algorithm takes advantage from the fact that the switches' turn-off moment overlaps with the peak of the converter output current. A single OC fault shrinks one of the peaks of the converter output current [69], as shown in Fig. 5.6.

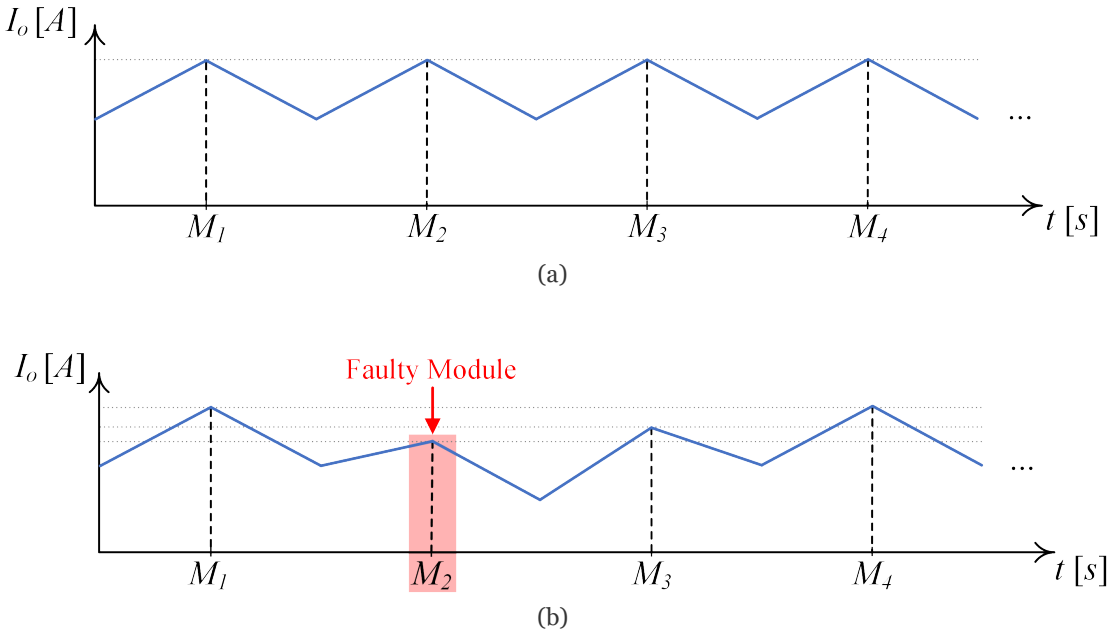


Fig. 5.6 Parallel-connected SAB converter output current evolution under: (a) healthy converter operation; (b) faulty operation, with fault in module 2. Labels of the x-axis identify the module producing each peak of the converter output current [69].

The simple act of evaluating the converter current amplitude might demonstrate ineffective in more complex converter topologies. To meet the requirements of reliable diagnostics in complex converter assemblies, more elaborated fault diagnostic algorithms have been developed. Resorting to the same diagnostic variable (converter input current), a fault diagnostic algorithm based on the sign of the current derivative can detect and identify OC faults in interleaved DC–DC converters [70]. The algorithm performs a comparison between the measured derivative sign and the expected derivative sign, on each interval considered in the analysis. As represented in Fig. 5.7, each switching period comprises 6 identical intervals. In the example provided there, the mismatch in the derivative sign occurs in interval (d) of period T_{sw_2}.

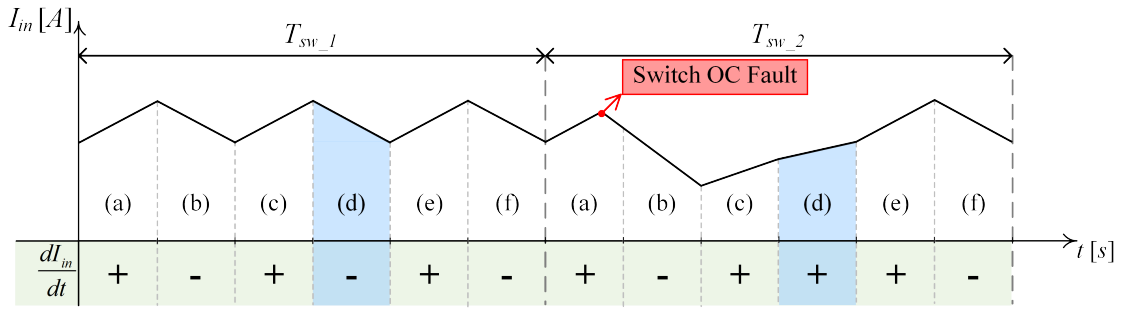


Fig. 5.7 Evolution in time of the three-phase interleaved DC–DC boost converter input current, over two switching periods (T_{sw_1} and T_{sw_2}). Shadowed intervals highlight the differences in the sign of dI_{in}/dt [70].

As one of the DC–DC converter topologies showing higher figures of merit for high-voltage and high-power applications, the modular multilevel converter (MMC) is a relatively complex DC–DC converter topology which gathers more interest. To assess the health state of the switches that compose each submodule of a MMC, an alternative fault diagnostic algorithm establishes a comparison between the voltages measured at the input and output of each submodule [71]. The algorithm is based on a modular architecture, meaning that each submodule of the MMC must contain all the sensing elements required to deploy the algorithm.

The voltage measured in any of the magnetic components (inductors or transformers) of a DC–DC converter provides a fault diagnostic solution with wide spectrum of action, allowing the diagnostic of switch faults in a plethora of converter topologies [72]–[74]. By cross-checking the information available in the voltage waveform and the gating signal(s) applied to the converter switch(es), it is possible to identify both OC and SC faults in the converter switch(es) [72]–[74]. Based on the fault signatures extracted from the magnetic components voltages, an alternative algorithm overrides the limitations manifested by the original algorithm, by improving the fault diagnostic capabilities for converters operating at DCM [75].

More elaborated DC–DC converters, as it is the case of the phase-shifted full-bridge (PSFB) converter, usually imply more specific and targeted fault diagnostic strategies. Aiming the diagnostic of SC faults in the primary side bridge of the PSFB converter [76], information is extracted from two converter variables: the input current and the transformer primary voltage. A SC fault in the primary-side bridge promotes a significant increment in the input current, far exceeding a predefined threshold, selected empirically [76]. To identify which one of those two switches is effectively faulty, the algorithm checks the transformer primary voltage waveform. This observation aims at finding the sign of the transformer primary voltage, as the position of the faulty switch affects its sign.

In the last few years, a couple of alternative, non-invasive strategies were presented in the literature, aiming standard and simple converter topologies. The diode voltage is

adopted as diagnostic variable in an alternative fault diagnostic algorithm, aimed at non-isolated DC–DC converters. The establishment of logical relations between the diagnostic variable and the converter gating signals enable the diagnostic of OC and SC faults in single-switch non-isolated DC–DC converters, not only in the converter switch, but also in the diode [77]. At least one additional voltage sensor is required to implement the algorithm. Meanwhile, improved iterations of the same strategy have been proposed by Givi *et al* [78], [79]. Both the diode and inductor voltages are acquired, allowing the prompt identification of faults on the semiconductors, capacitor, and inductor of non-isolated DC–DC converters [78]. To promote the adoption of non-invasive fault diagnostic functions for non-isolated single-switch DC–DC converters, a Rogowski coil sensor monitors the converter inductor voltage. Two important diagnostic actions are attainable concurrently, based on a single diagnostic variable: 1) determine the presence of switch faults in non-isolated single-switch DC–DC converters; and 2) monitor the condition of the converter capacitor, resorting to data of the equivalent series resistance (ESR) [79].

A distinctive approach, based on the second-order derivative of the converter input current, has been proposed to diagnose switch faults in bidirectional interleaved DC–DC converters [80]. The fault detection is obtained by checking the magnitude of the second-order discrete-time derivative of the converter left-side current in well-defined periods. To identify the faulty switch, information of the gating signals is cross-checked with the information of the second-order discrete-time derivative to locate the faulty switch [80].

DC–DC converters commonly rely on current control strategies employing PI controllers. Taking profit of such feature, an alternative diagnostic strategy based on the analysis of the reference current error was proposed in [81]. The abnormal increment of the reference current error provides good fault indicators, that enable the detection of power switches faults.

The literature also provides solutions that consider the particular architecture and behaviour of specific converter topologies, such as the hybrid Dickson converter. In [82], the fault diagnostic is achieved through the analysis of the voltage at the low-side switching node.

Latest research on condition monitoring of power electronics also focused on the development of strategies based on statistical analysis methods. Given the fact that these methods gather some converter variables and perform an evaluation of those variables over the time domain, this kind of methods can be considered to belong to the group of fault diagnostic algorithms using signal processing techniques over the time domain. For DC–DC converters, Jiang *et al.* [83] developed a fault diagnostic algorithm based on a Gaussian process regression and a genetic algorithm, employing it on a non-isolated buck converter.

5.1.1.2. Frequency-domain signal-processing-based algorithms

Fault diagnostic algorithms employing signal processing techniques in the frequency domain did not attract much attention of the scientific community involved in topics related to the improvement of availability of DC–DC converters. The significant computational effort and the large number of training sets usually required to recognise all switch fault events, constitute some of the hurdles for the successful implementation of such diagnostic algorithms.

The magnetic near field of the converter magnetic components (inductors or transformer) is used as fault diagnostic variable in one of the few examples of algorithms employing spectral analysis. The algorithm comprises the extraction of the information from the magnetic near field, through the computation of the Fast Fourier Transform (FFT) [84]. Auxiliary tools, based on neural networks and an accumulator, carry out the spectral analysis required to diagnose faults in the power switches, as depicted in Fig. 5.8.

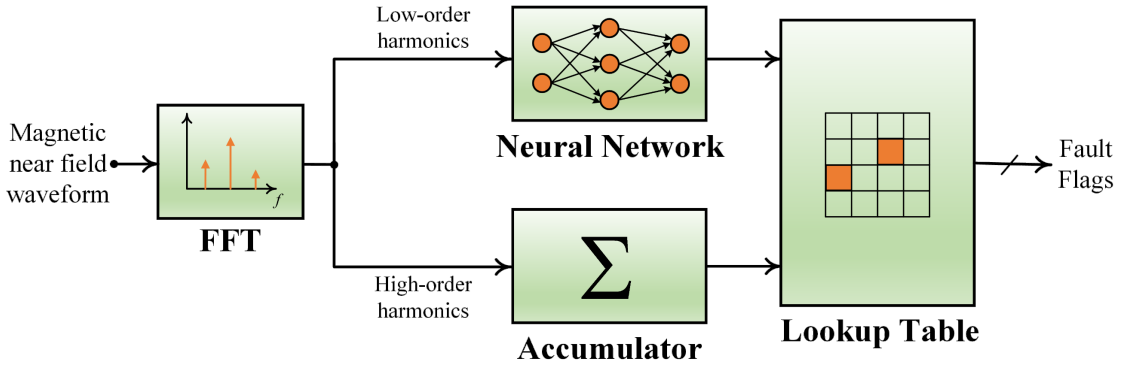


Fig. 5.8 Fault diagnostic algorithm based on the spectral analysis of the magnetic near field waveform.

A similar approach is adopted in [56], where the voltage of the magnetic components (inductor or transformer) of a multilevel DC–DC flying capacitor buck converter is sensed and analysed through the corresponding FFT.

In [85], failures on the switches of a synchronous boost converter are identified through the evaluation of the first-order harmonic of the radiated electromagnetic interference (EMI). The EMI is sensed through a dedicated antenna, placed next to the converter under evaluation, thus providing a non-invasive monitoring method, at the expense of a more complex and costly solution. Besides, the effectiveness of the method may eventually become compromised by other external EMI sources.

To determine the occurrence of semiconductor faults on interleaved DC–DC converters, the method proposed in [86] evaluates the magnitude and phase of the converter input current, focusing on the fundamental harmonic of the switching frequency. Within the group of fault diagnostic strategies deploying an analysis in the frequency

domain, the latter reveals as one of the methods requiring less computational and implementation effort.

5.1.2. Model-based fault diagnostic algorithms

Model-based fault diagnostic algorithms for DC–DC converters became popular in the last few years. As the implementation of these algorithms implies a relatively significant computational effort, the emergence of these algorithms was only made possible due to the increased processing capabilities of last-generation digital controllers.

These algorithms overcome part of the challenges faced by signal-processing-based algorithms, since model-based fault diagnostic algorithms feature resiliency and effectiveness while detecting OC and/or SC faults, regardless of the DC–DC converter operation conditions (e.g. switching frequency, load level, conduction mode, etc.). The robustness against non-linearities, such as noise or load transients, is also improved in model-based fault diagnostic algorithms.

To implement model-based fault diagnostic algorithms, a state-space model of the DC–DC converter under study must be established. Previous knowledge of the DC–DC converter parameters (inductances, capacitances, parasitic resistances, etc.) is a premise for the development of most model-based fault diagnostic algorithms.

In general terms, model-based algorithms aim to compare the expected converter response, modelled via analytical methods, with the effectively observed converter response, assessed through the analysis of the converter output signals such as voltage or current, as illustrated in Fig. 5.9. Based on detailed information about the converter parameters, the converter topology and the converter input signals, the converter behaviour is modelled and emulated with high degree of precision. Residuals are generated by comparing the converter response with the modelled response.

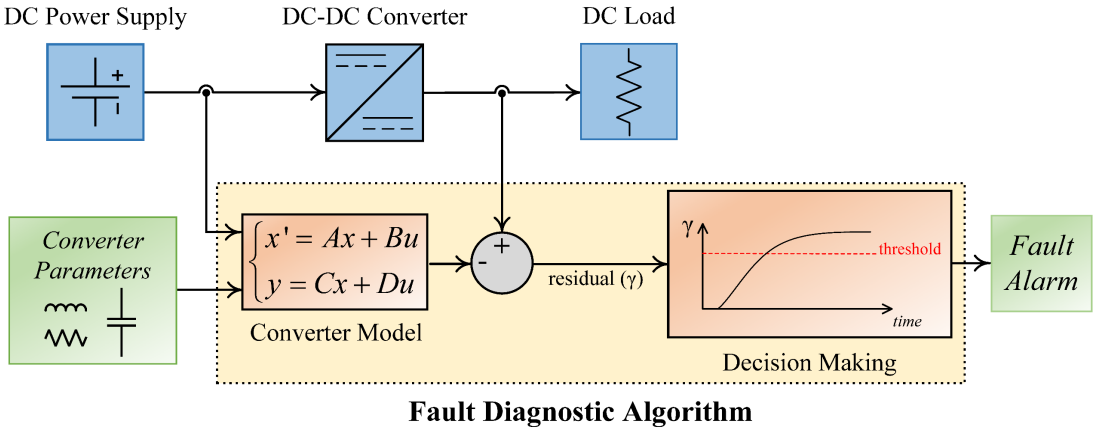


Fig. 5.9 Principles of implementation of a model-based fault diagnostic algorithm aimed at DC–DC converters.

A decision-making procedure, typically based on a careful evaluation, in the time domain, of the residual γ, allows to extract valuable information that give clues about the fault modes perturbing the converter operation. From the analysis made to the literature, it is concluded that model-based fault diagnostic algorithms suitable for DC–DC converters mainly differ between themselves regarding the strategies developed to estimate the converter response.

State observers are tools, within the group of model-based fault diagnostic algorithms, commonly adopted to estimate the state of DC–DC converters. The sliding mode observer is one of those tools. To obtain the estimation of the converter state using a sliding mode observer, the mathematical conditions that define the converter model are combined with the observer vectors [11], [87]:

$$x' = A\hat{x} + Bu + L\,\mathrm{sgn}(x - \hat{x}) \tag{5.1}$$

where $\hat{x}$ stands for the estimated state of variable x, L denotes the observer gains, and $\mathrm{sgn}(x - \hat{x})$ denotes the sign of the error between the measured and the estimated states. To ensure that sliding mode conditions are met, gains L should be set at very high values (in the order of thousands).

Sliding mode observers can be defined to estimate any converter variables, considered suitable for fault diagnostic purposes. Even though sliding mode observers were originally developed for MMCs, they can be also employed in DC–DC converters based on MMCs and related DC–DC converter topologies. Note that, depending on the converter topology and the selected diagnostic variables, this algorithm might not provide enough information to identify the faulty element, as indeed happens in MMCs [11], [87].

Relying on Luenberger observers to estimate the inductor current of an interleaved DC–DC boost converter, Zhuo *et al.* [88] employ such tool to detect and identify failures in any of the active switches of the converter. The robustness of the diagnostic results against parameter uncertainty and/or unexpected operation oscillations is further enhanced through the adoption of adaptive thresholds. This strategy is feasible for other converter topologies as well, but requires adaptations on the designed observer and, eventually, on the converter variables being observed.

Hu *et al.* [89] proposed an extended state observer to diagnose OC faults on a MMC. While the detection of the fault is supported by the information provided by the observer, the identification of the faulty switch also implies the evaluation of the capacitor voltage in each submodule.

Current emulation is one of the most recent strategies used to diagnose power switches faults in DC–DC converters [90], [91]. Diagnostic of both OC and SC fault events

in the switches of any non-isolated DC–DC converter topology is feasible. It is a fault diagnostic algorithm that establishes a short-term prediction of any desired converter variable, allowing to promptly detect abnormal deviations of that variable. In addition to the converter parameters, the converter input and output voltages, along with the inductor current, are the required diagnostic variables. The fault diagnostic action takes place in two steps. Faults are detected by comparing the expected inductor current for a moment and the measured inductor current at that same moment. According to the direction of the deviation between the measured and the expected inductor current, relevant information to identify the faulty component is obtained. This fault diagnostic algorithm provides an appropriate mean to diagnose switch faults in non-isolated DC–DC converters, allowing to identify such faults in a very short period of time. No additional sensors are required to deploy the algorithm.

Fault diagnosis based on a state estimator [10] demonstrates potential to extend the range of detectable failure modes, embracing faults occurring in sensors and passive components. Furthermore, the range of converter topologies compatible with this algorithm is very extensive [10]. During the fault detection stage, the residual resulting from the difference between the measured converter state and the estimated converter state is determined. A detection alarm is triggered if the Euclidean norm of the residual surpasses a predefined fault detection threshold. That threshold is defined empirically, based on a worst-case scenario, where the transients on voltage and current considerably increase the Euclidean norm of the residual. The fault identification stage is developed separately. It comprises the computation of the inner product between residual and each one of the fault signatures, available on a pre-established library. Note that the model estimator must be executed in real-time, at a very high sampling rate, thus demanding a significant computational effort. A fast and powerful DSP platform is, therefore, required to deploy the algorithm. This fact can be considered the major drawback of the algorithm. Conversely, the wide applicability, high resilience, and fast response represent the major virtues of this fault diagnostic algorithm.

Even though the diagnostic of power switches faults represents the majority of the research efforts developed so far, concerning the improvement of availability of DC–DC converters, the literature provides additional model-based algorithms that were developed with alternative purposes. These algorithms are typically employed in the estimation of converter parameters like inductances and capacitances. Still, these algorithms demonstrate potential to carry out fault diagnostic actions in power switches as well. These model-based algorithms also provide a solid framework for the future development of fault prognostic tools. For reference, a small sample of model-based algorithms aiming the

estimation of other converter states is provided: algorithms based on Kalman filters [92], self-tuned Kalman filters [93], observers featuring adaptive estimation of parameters [94], or adaptive gradient descent [95].

5.2. Proposed fault diagnostic strategies

Considering the evaluation to the scientific literature described in Section 5.1, it is clear that state-of-the-art fault diagnostic strategies are not handily nor attractive for implementation in simple power conversion solutions, namely those required for small-scale DC microgrids, deployed at homes and offices.

Following sub-sections describe alternative fault diagnostic strategies that aim to answer to the challenges of simplicity, low implementation effort, and effectiveness.

5.2.1. General Appliances

The evaluation of the non-isolated unidirectional interleaved boost converter and its operation principles (refer to Section 4.1.1) revealed that the converter input current (I_{in}) is perturbed in the presence of OC faults on the converter switches. More particularly, the analysis of the I_{in} derivative provides valuable information about the condition of the converter, suitable for fault diagnostic purposes. Unfortunately, the computation of the derivative involves a significant computational effort and, consequently, a higher implementation cost. Alternatively, the analysis of the amplitude of I_{in} along well-defined intervals, provides an effective tool to diagnose OC faults. Since the waveform of I_{in} might be corrupted by noise, load oscillations, and other non-linear events, it is important to deploy strategies capable of improving the robustness against unexpected perturbations. Simple mathematical operations allow to greatly improve the resiliency of the diagnostic process, without compromising its simplicity. Using I_{in} and the PWM signals together, a trivial solution can be used, consisting of the comparison between the absolute magnitude of I_{in} sensed at the rising edge of a PWM signal and the absolute magnitude of I_{in} sensed at the subsequent PWM falling edge.

Each rising edge establishes the beginning of each interval considered for the fault diagnostic procedure and, at the same time, identifies the switch to which the analysis is applied. For instance, the evolution of I_{in} along any interval starting with a rising edge of PWM signal q_1 provides useful information to diagnose faults of IGBT Q_1.

Right after acquiring the two samples of I_{in}, a logical relation is established between them. Under healthy condition, the sample taken at the rising edge should be equal or smaller than the sample taken at the subsequent falling edge:

$$I_{in}(\text{rising}) \leq I_{in}(\text{falling}) \tag{5.2}$$

This evaluation should be repeated, along one switching period, for as much times as the number of converter phases, to obtain information for each one of the converter phases. In this work, the evaluation shall be performed for three times within one switching period.

In the presence of an OC fault, it is observed that the sample taken at the rising edge of the PWM signal related to the faulty switch is higher than the sample taken at the subsequent falling edge:

$$I_{in}(\text{rising}) > I_{in}(\text{falling}) \tag{5.3}$$

According to (5.3), the presence of an OC fault can be detected by subtracting the samples taken at the falling edge instant and at the previous rising edge instant:

$$\Delta I_{in} = I_{in}(\text{falling}) - I_{in}(\text{rising}) \tag{5.4}$$

If ΔI_{in} is positive (i.e., I_{in} increases in the time period under analysis), the switch associated to that converter phase is healthy. In opposition, if ΔI_{in} is negative, I_{in} decreases, which means that an OC fault has occurred in the switch of that converter phase.

Nevertheless, the analysis of the sign of ΔI_{in}, by itself, does not provide sufficiently resilient diagnostic results, particularly when non-linearities like load transients or high-frequency noise impact the converter operation. To overcome such hurdle, the diagnostic variable is normalised, according to the following expression:

$$\Delta I_{in_{norm}} = \frac{\Delta I_{in}}{\max(\Delta I_{in})} \tag{5.5}$$

where $\Delta I_{in_{norm}}$ denotes the normalised diagnostic variable, ΔI_{in} refers to the oscillation of the converter input current for the interval under analysis, and $\max(\Delta I_{in})$ denotes the maximum oscillation of the converter input current. Please note that $\max(\Delta I_{in})$ is memorised in the diagnostic system and is continuously evaluated. Every time that ΔI_{in} is computed, its value is compared with the value of $\max(\Delta I_{in})$, which is stored in the memory of the diagnostic system. In case that ΔI_{in} surpasses $\max(\Delta I_{in})$, the value of $\max(\Delta I_{in})$ stored in memory is replaced by ΔI_{in}. Also note that $\Delta I_{in_{norm}}$ is the generic denomination of the three diagnostic variables, assigned to each one of the converter switches. The three diagnostic variables are denoted as ΔI_1, ΔI_2, and ΔI_3, and result from the application of (5.5) during the periods of interest for their computation. For instance, ΔI_1 is computed resorting to the evaluation of I_{in} within the period comprised between the rising edge of the gating signal q_1 and the subsequent falling edge. Each diagnostic variable (ΔI_1, ΔI_2, and ΔI_3) is computed only once for every switching cycle.

Under healthy condition, the diagnostic variables $\Delta I_{in_{norm}}$ of all converter phases should remain, in theory, unchanged and equal to 1, regardless of the load level or switching frequency. As a result of an OC fault, at least one of the three diagnostic variables (ΔI_1, ΔI_2, or ΔI_3) becomes negative.

To accommodate non-linearities and, at the same time, ensure the effectiveness of the proposed strategy, a threshold equal to –0.5 is defined as criterion for issuing a fault alarm:

$$\Delta I_{in_{norm}} < -0.5 \rightarrow \text{OC fault} \tag{5.6}$$

In case of simultaneous conduction of multiple converter phases (i.e., when the switching duty cycle surpasses 1/3), it is expected that two of the diagnostic variables will concurrently decrease below the selected threshold, as a result of the OC fault. Such observation results from the fact that the faulty switch impacts the measured ΔI_{in} in multiple intervals. Therefore, a fault identification strategy is implemented to distinguish the faulty switch. Right after triggering the fault alarm, the fault identification strategy checks which of the gating signals was active for a longer period of time prior the moment of activation of the fault flag.

To obtain effective diagnostic results, it must be ensured that the converter input current is sampled at the instants of transition between switch states. The selected sampling rate should meet the following condition:

$$f_s \geq 2nf_{sw} \tag{5.7}$$

where f_s denotes the sampling rate, n denotes the number of converter phase, and f_{sw} denotes the switching frequency. Since the sampling moments occur at the instants of transition between switch states, the coordination of the sampling procedure is quite straightforward and easy to synchronise.

Based on (5.7), the sampling rate of the converter input current solely depends on the switching frequency and on the number of converter phases. On the other hand, the switching duty cycle D does not have influence on the minimum sampling rate f_s required to obtain accurate diagnostic results.

Along with the improved diagnostic capability over a wide range of load levels, conduction modes, and switching frequencies, the normalisation of the diagnostic variables also prevent the misdiagnosis of semiconductor faults when the duty cycle D approaches or equals either 1/3 or 2/3.

Furthermore, this strategy provides good diagnostic results in a relevant range of switching frequencies, as it is demonstrated further ahead. Its effectiveness is confirmed for the converter operation up to 5 *kHz*, which is a common range of switching frequencies adopted in converters based on the IGBT technology.

5.2.1.1. Simulation results

The effectiveness of the fault diagnostic strategy was validated theoretically through a dedicated simulation model, developed in *Simulink™* environment. The configuration of the model, along with the adopted parameters are described with detail in Appendix A.1.

In all simulated scenarios, OC fault conditions of IGBT Q_1 are considered. Fig. 5.10 depicts the evolution of the three fault diagnostic variables $\Delta I_{1...3}$, used as the reference to diagnose faults in converter IGBTs, for two distinctive output voltage levels. Each of the diagnostic variables is associated to a specific IGBT of the converter. In this case, the diagnostic of a failure in IGBT Q_1 takes place by monitoring the variable ΔI_1.

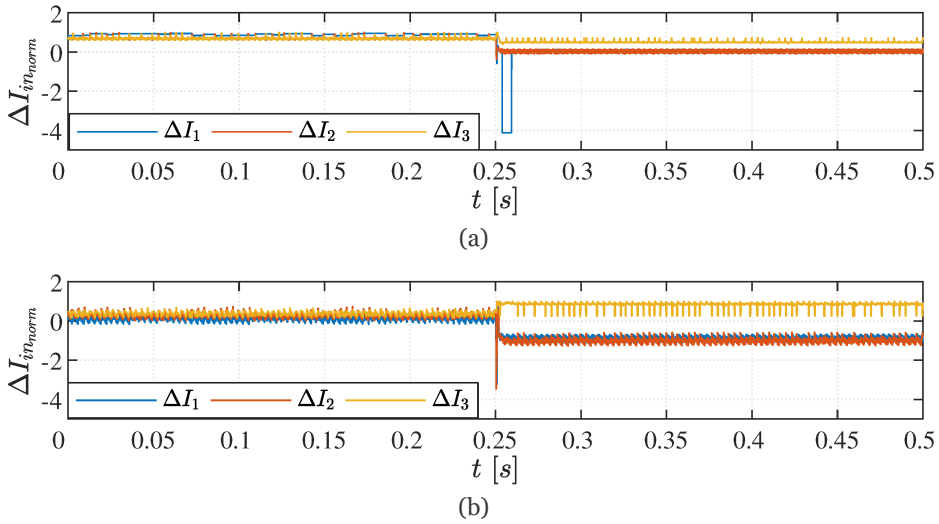


Fig. 5.10 Evolution in time of the fault diagnostic variables $\Delta I_{1...3}$, observed in case of an OC fault on IGBT Q_1, taking place at $t = 0.25012\ s$. Two distinctive output voltage levels are considered: (a) $V_{out} = 39\ V$; (b) $V_{out} = 60\ V$. The converter switching frequency f_{sw} is 3 kHz.

The proposed fault diagnostic algorithm demonstrates excellent capability to correctly diagnose faults, regardless of the converter output voltage, as shown in Fig. 5.10. Right after the OC fault, a distinctive depreciation of the diagnostic variable ΔI_1 takes place. Regarding the condition $V_{out} = 39\ V$, represented in Fig. 5.10 (a), it is stated that only the diagnostic variable ΔI_1 surpasses the threshold defined for issuing a fault alarm. For the condition $V_{out} = 39\ V$, the duty cycle D is set below 1/3, meaning that there is no overlap on the conduction of the converter phases and, consequently, only one of the diagnostic variables decreases below the threshold. As for the second scenario, when the output voltage is equal to 60 V – Fig. 5.10 (b) – it is interesting to note the simultaneous depreciation of two diagnostic variables (ΔI_1 and ΔI_2). Such behaviour is explained by the operation region of the converter. In this scenario, the duty cycle of the switching commands lies within the region $1/3 < D < 2/3$, meaning that there are periods of overlap on the conduction of two phases of the converter. In this particular case, it is the temporary overlap on the conduction of IGBT Q_1 and IGBT Q_2 that induces the concurrent depreciation of ΔI_1 and ΔI_2.

According to the results shown in Fig. 5.11 (a), which provides a zoomed view of the results shown in Fig. 5.10 (a), only the diagnostic variable ΔI_1 surpasses the threshold, 0.58 *ms* after introducing the fault. Regarding the second scenario, represented in Fig. 5.11 (b), both ΔI_1 and ΔI_2 become negative and surpass the threshold. The diagnostic variable ΔI_1 is the first one to decay, surpassing the defined threshold 0.2 *ms* after introducing the fault – representing 60 % of the switching period.

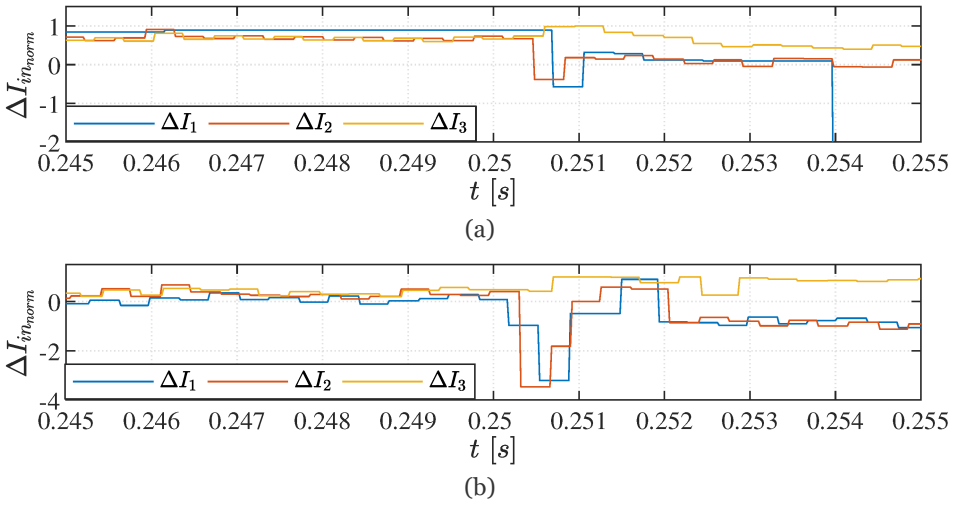


Fig. 5.11 Zoomed view of the results depicted in Fig. 5.10: (a) V_{out} = 39 *V*; (b) V_{out} = 60 *V*.

The fault diagnostic strategy also shows the ability to correctly diagnose faults at several switching frequencies. Fig. 5.12 depicts the fault diagnostic variables $\Delta I_{1...3}$ in the event of variation of the switching frequency.

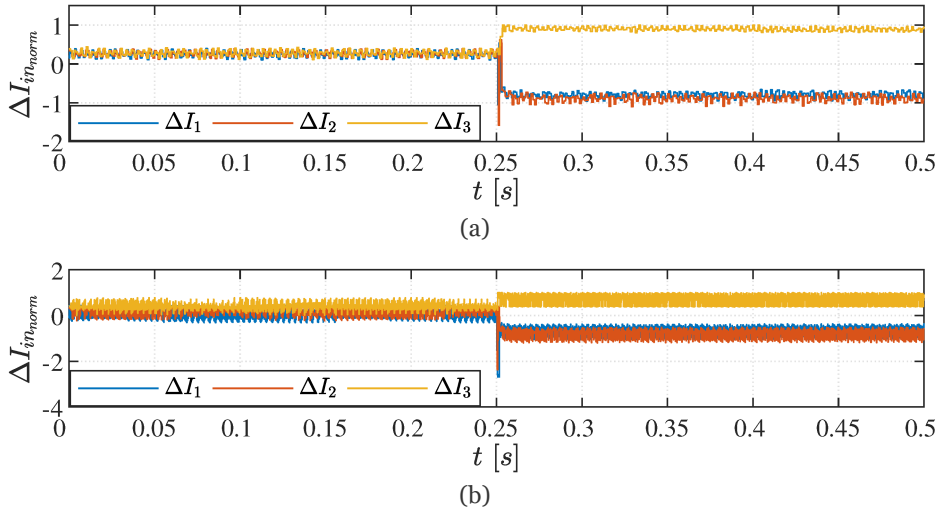


Fig. 5.12 Evolution in time of the fault diagnostic variables $\Delta I_{1...3}$, when an OC fault occurs in IGBT Q_1, at t = 0.25024 *s*. Two distinctive switching frequencies f_{sw} are considered: (a) f_{sw} = 1 *kHz*; (b) f_{sw} = 5 *kHz*. The output voltage V_{out} is 60 *V*.

Given the output voltage considered in the tests – V_{out} = 60 *V* – the duty cycle *D* lies within the region 1/3 < *D* < 2/3, meaning that there is temporary overlap on the conduction of two phases. As a result, it is observed that both diagnostic variables ΔI_1 and ΔI_2 decay

below the defined threshold. Such statement is valid for the scenario depicted in Fig. 5.12 (a), concerning the operation at 1 *kHz*, as well as for the scenario depicted in Fig. 5.12 (b), concerning the operation at 5 *kHz*.

Fig. 5.13 provides a zoomed view of the fault diagnostic variables $\Delta I_{1...3}$ in case of adoption of distinctive switching frequencies.

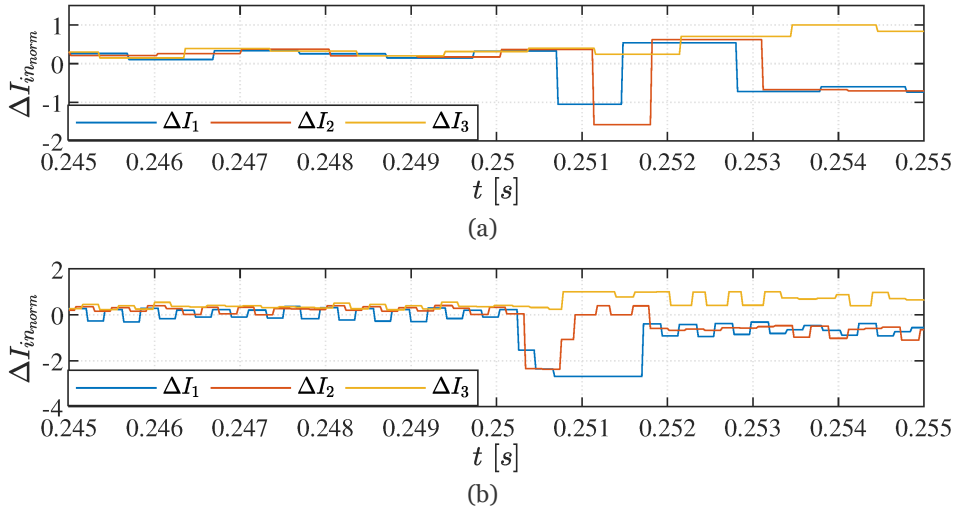


Fig. 5.13 Zoomed view of the results depicted in Fig. 5.12: (a) f_{sw} = 1 *kHz*; (b) f_{sw} = 5 *kHz*.

Regarding the converter operation at 1 *kHz* – Fig. 5.13 (a) – it is observed that the diagnostic variable ΔI_1 is the responsible for triggering the fault alarm. The threshold is surpassed 0.48 *ms* after introducing the OC fault, meaning that the diagnostic is achieved in half of the switching period.

Considering the converter operation at 5 *kHz* – Fig. 5.13 (b) – the diagnostic variable ΔI_1, which was predominantly positive in the pre-fault period, becomes negative and surpasses the defined threshold 0.02 *ms* after introducing the fault. The identification of IGBT Q_1 as the faulty switch occurs 0.08 *ms* later. All the diagnostic procedure takes place in less than two switching periods.

To check the resiliency of the fault diagnostic method against load fluctuations, a scenario of harsh load variation is simulated. A step variation of the converter output voltage is introduced at t = 0.25 *s*. At that moment, the load voltage V_{out} is reduced from 60 *V* to 30 *V*. As a result of the load transient, the converter input current I_{in} drops to 1/4 of its original value, in less than 1 *ms*. Later, at t = 0.50036 *s*, an OC fault is introduced in IGBT Q_1. The overview of the input current I_{in} and the three diagnostic variables (ΔI_1, ΔI_2, and ΔI_3) is depicted in Fig. 5.14, while a zoomed view is provided in Fig. 5.15.

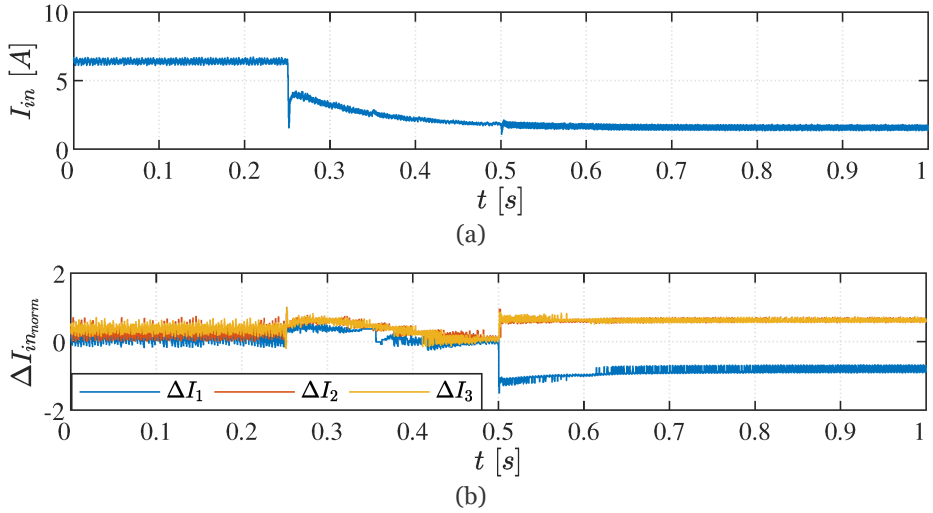


Fig. 5.14 (a) Evolution in time of the converter input current I_{in}; (b) Evolution in time of the fault diagnostic variables $\Delta I_{in_{norm}}$, considering a load transient scenario. The load transient, imposed at t = 0.25 *s*, is followed by an OC fault in IGBT Q_1, at t = 0.50036 *s*. The converter switching frequency f_{sw} is 3 *kHz*.

Referring to Fig. 5.14, it is perceived that there is a clear superposition of all the three diagnostic variables, while the healthy condition prevails. As a result of the load transient condition, minimal shift occurs on all three diagnostic variables. Indeed, all three diagnostic variables show a minor increase right after the load transient. Later, a distinctive and significant depreciation of the variable ΔI_1 takes place, right after the OC fault, while variables ΔI_2 and ΔI_3 remain positive and assume values near to 1.

Fig. 5.15 provides a clear view of the three diagnostic variables, at the moment at which the OC fault takes place.

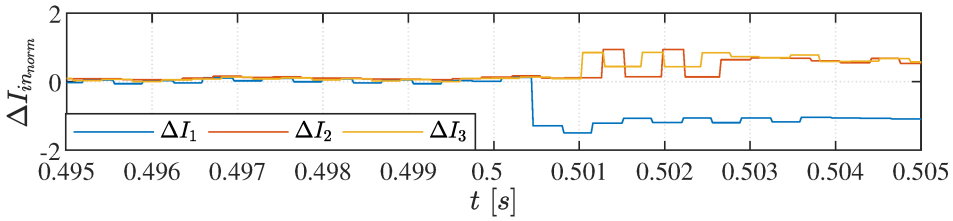


Fig. 5.15 Zoomed view of the results depicted in Fig. 5.14.

The transient on the converter output voltage did not generate a false alarm. Only the OC fault induced a transition to negative values of the diagnostic variable ΔI_1, 0.1 *ms* after the OC fault.

5.2.1.2. Experimental results

To validate the simulation results presented in Section 5.2.1.1, operation scenarios similar to those adopted in simulation were replicated in experimental context. The architecture and parameters of the laboratory prototype are described with detail in Appendix B.1.

Fig. 5.16 depicts the behaviour of the fault diagnostic variable ΔI_1 for two distinctive output voltage levels.

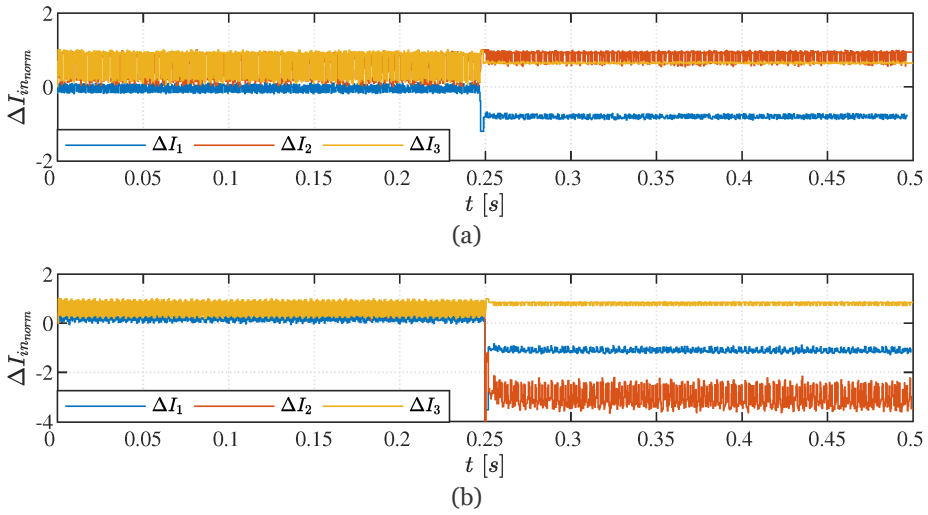


Fig. 5.16 Evolution in time of the fault diagnostic variables $\Delta I_{1...3}$, observed in case of an OC fault on IGBT Q_1, taking place at $t = 0.24950\ s$. Two distinctive output voltage levels are considered: (a) $V_{out} = 39\ V$; (b) $V_{out} = 60\ V$. The converter switching frequency f_{sw} is 3 *kHz*.

The proposed fault diagnostic algorithm demonstrates excellent capability to correctly diagnose faults under different output voltage levels, as shown in Fig. 5.16. These results put into evidence the capability of the strategy to deal with various load levels and conduction regimes. Right after the OC fault, there is a distinctive oscillation of the diagnostic variable ΔI_1. The diagnostic variable, which was predominantly positive before the fault, has a sharp transition to negative values right after the fault, allowing for a fast diagnostic action. In both scenarios depicted in Fig. 5.16, the diagnostic is completed in less than 0.4 *ms*, corresponding to 1.2 switching periods. It is also worth noting that the results of Fig. 5.16 have a pretty good match with the corresponding simulation results, provided in Fig. 5.10.

For the condition of $V_{out} = 60\ V$ – refer to Fig. 5.16 (b) – it is observed that both ΔI_1 and ΔI_2 drop below the defined threshold. Such behaviour takes place due to particular operation condition of the converter. Given the temporary overlap, in time, on the conduction of IGBTs Q_1 and Q_2, the OC fault will affect the two diagnostic variables, as previously stated in Section 5.2.1.1. Such behaviour does not impact the accuracy nor the effectiveness of the fault diagnostic task.

Correct and quick fault diagnostic results are also verified for distinctive switching frequencies, as shown in Fig. 5.17.

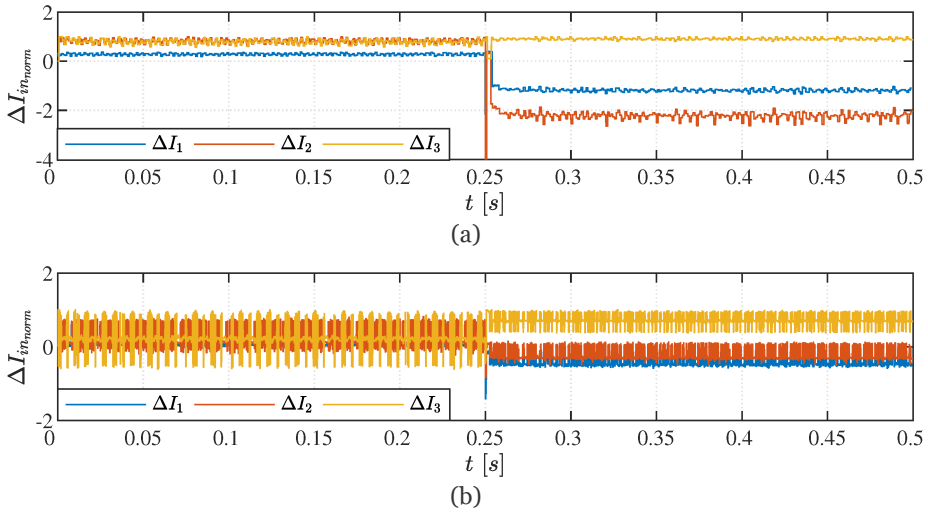


Fig. 5.17 Evolution in time of the fault diagnostic variables $\Delta I_{1...3}$, observed in case of an OC fault on IGBT Q_1, taking place at $t = 0.25024$ s. Two distinctive switching frequencies f_{sw} are considered: (a) $f_{sw} = 1$ kHz; (b) $f_{sw} = 5$ kHz. The converter output voltage V_{out} is 60 V.

The sharp transition of the diagnostic variable ΔI_1 to negative values occurs right after the fault, surpassing the defined threshold. In both cases, the diagnostic procedure is completed in less than 0.2 ms, corresponding to 1/5 of a switching period (for $f_{sw} = 1$ kHz), and to 9/10 of a switching period (for $f_{sw} = 5$ kHz). The adopted output voltage implies that the switching duty cycle lies within the region $1/3 < D < 2/3$. As described in Section 5.2.1.1, such fact implies the concurrent depreciation of two diagnostic variables – for the scenarios presented in Fig. 5.17, the depreciation occurs in the diagnostic variables ΔI_1 and ΔI_2.

One of the challenges faced by multiple fault diagnostic algorithms available in the literature concerns the correct diagnostic of faults when the duty cycle of the converter gating signals approaches to 1/3 and 2/3. By adopting the fault diagnostic strategy, such challenge is pretty well addressed, as shown in Fig. 5.18. False fault alarms are avoided in an effective manner.

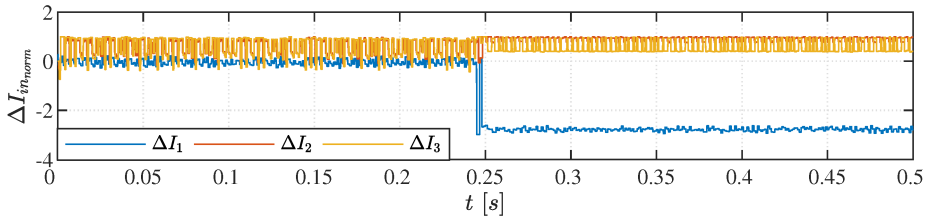


Fig. 5.18 Evolution in time of the fault diagnostic variables $\Delta I_{1...3}$, observed when the duty cycle of the converter gating signals equals 1/3. An OC fault occurs in IGBT Q_1, at $t = 0.24474$ s. The converter switching frequency f_{sw} is 1 kHz.

As demonstrated in Fig. 5.18, the three diagnostic variables remain positive under healthy converter condition. Only the OC fault introduces a relevant decrement of the diagnostic variable ΔI_1, while the other two diagnostic variables remain positive. The diagnostic procedure is completed in 0.26 ms, corresponding to 26 % of a switching period.

Chapter 6

Fault tolerance in DC–DC converters

Fault diagnosis assumes pivotal importance in the sense of promoting high availability standards for power electronics converters, namely DC–DC converters, through the detection and identification of failures in critical components. Still, fault diagnostic actions do not allow, by themselves, to banish neither smooth the negative side-effects of faults in those converters. Implementation of modifications on either the converter (hardware) or control (software) of faulty DC–DC converters enables the continuous power conversion function, with good quality levels, along the post-fault period. Those modifications, introduced on the hardware and/or control of faulty DC–DC converters, are usually termed as reconfiguration strategies.

Naturally, the adoption of reconfiguration strategies does not allow, in most cases, to fully recover the power conversion capabilities of a DC–DC converter nor the original power quality observed prior to the fault. Power quality degradation and derating of the power transferred to the load are commonly observed, even after the reconfiguration of the faulty DC–DC converter. Side effects should be expected as a result of the implementation of the reconfiguration strategies. Higher conduction and switching losses are two good examples of the side effects that are commonly experienced during the post-fault operation of a converter implementing reconfiguration strategies. As a result, the design of reconfiguration strategies should carefully consider, among others, the aspects of efficiency, potential impact on the converter lifetime, and cost effectiveness.

This chapter is structured as follows. Firstly, a careful analysis to the state-of-the-art reveals the currently existing reconfiguration strategies and their target DC–DC converter topologies. The presentation of the state-of-the-art is complemented with a critical evaluation of the pros and cons of each reconfiguration strategy. Then, the novel fault-tolerant DC–DC converter topologies (hardware) and control reconfiguration strategies (software) developed in the framework of this work are presented and detailed. Finally, simulation and experimental results are provided, aiming a careful evaluation of the proposed contributions and their advantages over existing ones. Following the methodology adopted in Chapter 5, each section focuses on the fault-tolerant DC–DC converter topologies and control reconfiguration strategies suitable for each application – EV charging, LED lighting and general appliances.

6.1. State-of-the-art fault tolerance strategies

The state-of-the-art on fault tolerance strategies aimed at DC–DC converters provides a reasonable set of solutions, covering a wide range of converter topologies [49], [50]. To obtain fault-tolerant operation of a power converter, it is generally required to apply modifications on the hardware and/or software (i.e., the converter controller) of DC–DC converters. For that reason, it is commonly mentioned that fault tolerance implies the adoption of reconfiguration strategies. These strategies may be classified according to the hardware requirements and to the changes adopted in the control strategies to assure smoother operation.

Based on the requirements for implementing each reconfiguration strategy, it is possible to establish classification criteria for the fault tolerance strategies available in the literature, as stated in the schematic presented in Fig. 6.1.

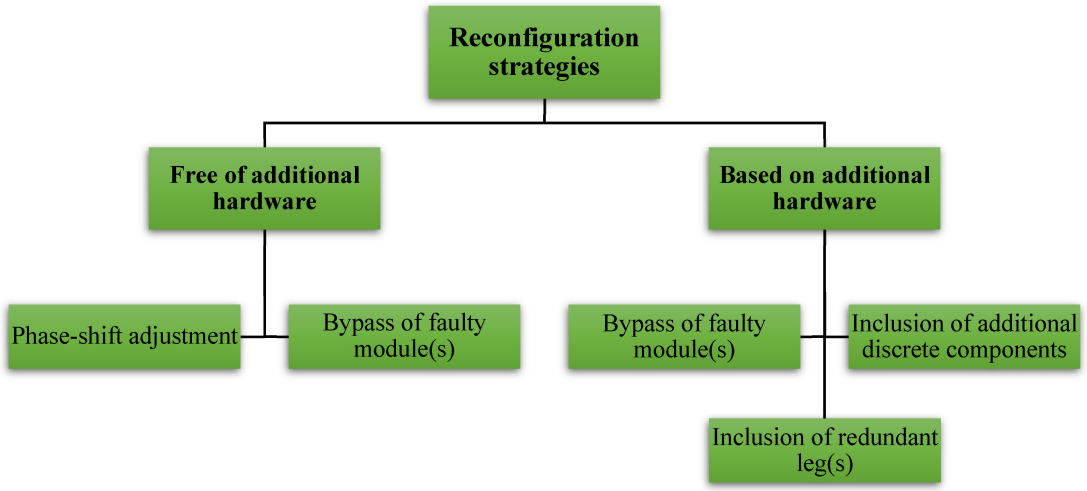


Fig. 6.1 Classification of the reconfiguration strategies, aimed at DC–DC converters, available in the scientific literature.

In this work, the reconfiguration strategies are classified according to their requirements in terms of hardware. With regards to the reconfiguration strategies obviating additional hardware, two categories are established: phase-shift adjustment and bypass of faulty module(s). As for the reconfiguration strategies implying additional hardware for their adoption, three distinctive groups are defined: bypass of faulty module(s), inclusion of redundant leg(s), and inclusion of additional discrete components.

It is noted that there is not a universal criterion for the classification of the reconfiguration strategies; other criteria are valid as well and are documented in the scientific literature [96], [97].

Following sub-sections detail each reconfiguration strategy, providing a generic explanation about the principles of implementation, along with some references to the literature that deal with such reconfiguration strategies.

6.1.1. Reconfiguration strategies free of additional hardware

It is possible to find a significant set of DC–DC power conversion solutions which take advantage of the inherently fault-tolerant architecture of some converter topologies to maintain the power conversion function during the post-fault period, without resorting to any additional hardware. Most common reconfiguration strategies free of additional hardware are based on two distinctive approaches: phase-shift adjustment and bypass of the faulty module(s).

Even though the majority of the reconfiguration strategies free of additional hardware fit into the two aforementioned approaches, there are few alternative approaches that rely on the distinctive nature and architecture of certain power conversion solutions, designed to meet the needs of particular practical applications, to naturally achieve fault tolerance. It is the case of the power conversion systems proposed in [98], [99], based on cascaded DC–DC converters, which are targeted at renewable energy systems integrating energy storage capability.

6.1.1.1. Phase-shift adjustment

Fault-tolerant control strategies based on phase-shift adjustment introduce changes in the modulation of the gating signals applied to the faulty converter. This reconfiguration measure implies the adjustment of the phase-shift between the control signals applied to the healthy converter switches/modules (Fig. 6.2).

After identifying a fault which impairs the switch controlled by signal q_1, the gating signal related to the faulty switch is eliminated from the switching pattern. Also, the phase-shift between gating signals applied to the healthy switches is corrected, taking into account the number of switches which remain intact. In the example shown in Fig. 6.2 (b), where phase-shift adjustment is considered, gating signals q_2 and q_3 are shifted by π rad between each other, after $t = 4\pi\ rad$. By adopting this reconfiguration strategy, the symmetry of the interleaved switching pattern is re-established for the post-fault period.

Phase-shift adjustment is a reconfiguration measure commonly adopted in converter topologies that employ a phase-shift modulation strategy. Therefore, phase-shift adjustment provides fairly good results not only on multi-phase converters, also known as interleaved DC–DC converters [67], [70], [86], [100]–[105], but also on dual active bridge (DAB) converters [106], [107], parallel-connected SAB DC–DC converters [69], input-parallel output-series (IPOS) converters [108], modular converters with hybrid Dickson cells [109], or flyback-forward modular converters [110]. In the case of interleaved DC–DC converters, phase-shift adjustment is sometimes complemented with other reconfiguration

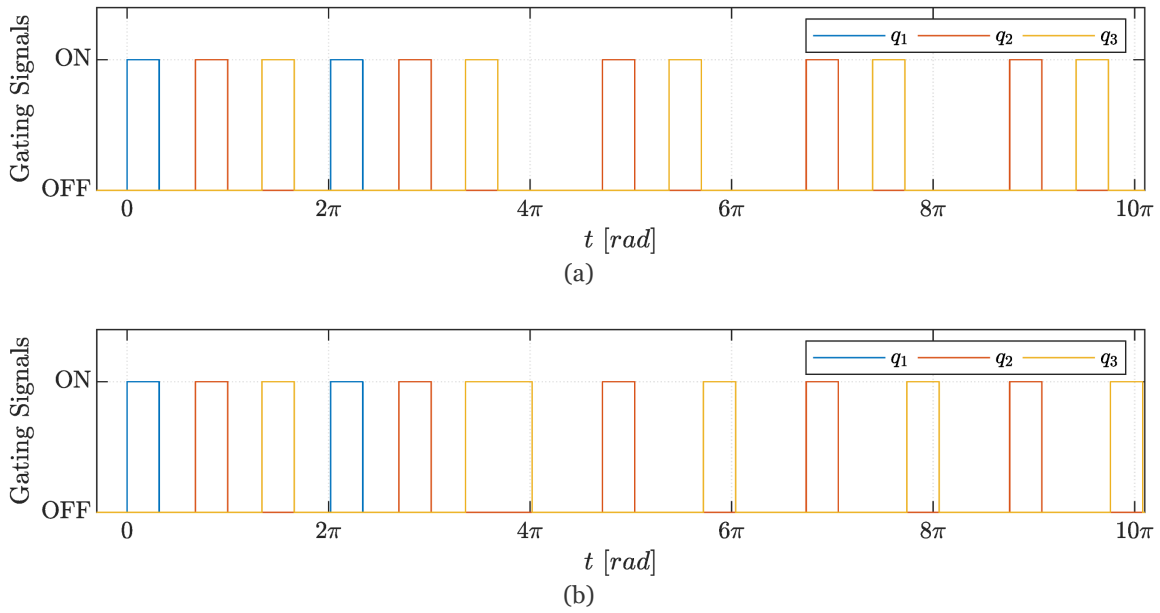


Fig. 6.2 Evolution of a typical interleaved switching pattern, observed after an OC fault occurring at the beginning of the third switching period ($t = 4\pi$ *rad*): (a) without reconfiguration; (b) with phase-shift adjustment.

measures, as for instance current reference adjustment [86], [104], aiming to provide enhanced balance between the converter phases. For SAB and DAB converters, phase-shift adjustment is usually employed in conjunction with isolation of the entire faulty leg [106], [107].

Simplicity, low or null implementation cost, effectiveness, and the broad applicability are the major benefits of this fault-tolerant control strategy. Nonetheless, a lower power conversion efficiency ratio should be expected, as a result of the implementation of this reconfiguration strategy. In addition, the deployment of phase-shift adjustment is often associated to increased stress on the healthy components of the reconfigured converters.

6.1.1.2. Bypass of faulty module(s)

Albeit uncommon, the implementation of bypass functions may take place in a very simplified manner in certain modular converter topologies. The original structure of the converter includes all the components required to perform the bypass function. Such approach may be considered in power conversion solutions with a modular architecture, relying on conventional DC–DC converters to build each module [111]–[113]. It can be also considered for the modular multilevel DC–DC converter proposed in [114], [115], depicted in Fig. 6.3.

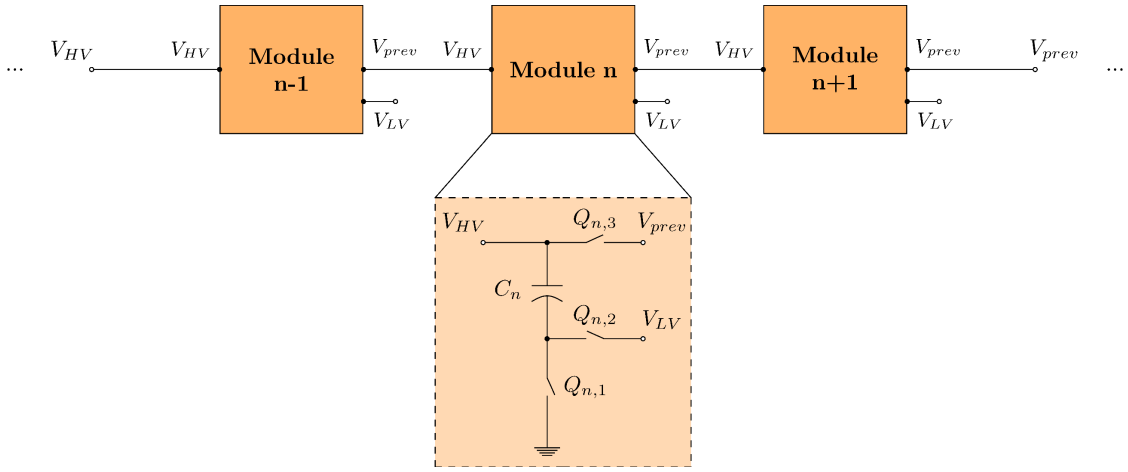


Fig. 6.3 Fault-tolerant bidirectional modular multilevel converter [114], [115].

For the aforementioned converter configurations, the implementation of the reconfiguration strategy is restricted to modifications on the control of the switches of the bypassed module. Such modifications usually consist of turning off all the components of the faulty module and enabling the element with bypass function.

Thanks to the architecture of some input-parallel-connected converters, as it is the case of the IPOS converters presented in [116], fault tolerance is naturally achieved, and the bypass of faulty module(s) takes place automatically, without requiring any modifications on hardware neither software.

Bypassing the faulty module(s) of a modular DC–DC converter topology presents some advantages over identical reconfiguration strategies: 1) the implementation cost is null; and 2) the transition to the fault-tolerant control strategy does not imply relevant changes in the original control scheme.

On the other hand, the bypass of the faulty module(s) also brings in limitations. Usually, the power conversion capabilities of the converters employing such reconfiguration strategy suffer a considerable depreciation along the post-fault period.

6.1.2. Reconfiguration strategies implying additional hardware

The group of reconfiguration strategies implying additional hardware encompasses most reconfiguration strategies available in the literature. Additional components are introduced in the original converter architecture, in a way that enables the most prolific exploitation of the converter capabilities, aiming to partially recover the power conversion capabilities lost as a result of OC and/or SC semiconductor faults. Typically, the inclusion of additional components aims to either bypass the faulty element, if the converter has a modular architecture, or to directly replace that element. Such replacement can take place at the device level – e.g. single triode for alternating current (TRIAC), IGBTs, MOSFETs –

or at the leg level – e.g. redundant half-bridge – depending on the DC–DC converter topology under consideration.

6.1.2.1. Bypass of faulty module(s)

In modular DC–DC converter topologies whose original architecture does not provide enough elements to develop bypass functions, it becomes necessary to introduce additional discrete components, aiming to obtain fault tolerance capabilities. It is the case of the input-series output-series/parallel (ISOSP) converter [119], the cascaded H-bridge converter [120], the hybrid bidirectional DC–DC converter [121], or the input-series output-parallel (ISOP) converter [116]–[118], where the faulty module is bypassed resorting to additional components, such as thyristors or solid-state relays (SSRs), following the configuration shown in Fig. 6.4. Each module represents any simpler DC–DC converter topology.

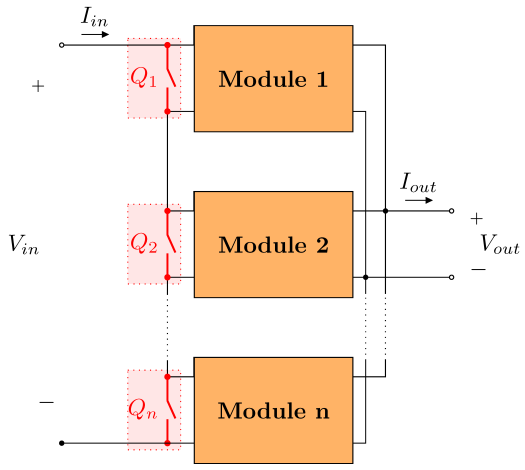


Fig. 6.4 Fault-tolerant ISOP converter [117], [118]. Shaded areas delimited by dashed lines highlight the bypass switches, denoted as Q_1, Q_2, and Q_n.

Fault tolerance based on bypass of faulty modules is equally feasible on cascaded DC–DC converters [122]. Due to the cascaded configuration, a single switch fault may compromise the power conversion function of the entire converter. Under such circumstances, the isolation and bypass functions assume major importance. To obtain the isolation and bypass of the potential faulty module(s), a significant number of additional power switches must be included in the fault-tolerant cascaded DC–DC converter, in order to cover all potential failure modes. Fig. 6.5 depicts a fault-tolerant cascaded converter, highlighting the components required to reconfigure the converter operation.

Reconfiguration strategies based on the bypass of faulty module(s) provide important advantages over other reconfiguration strategies, especially thanks to the minimal modifications imposed on the post-fault control. On the other hand, the cost of implementation and degree of complexity of the hardware structure are the main drawbacks commonly related to the reconfiguration strategies based on the bypass of faulty module(s).

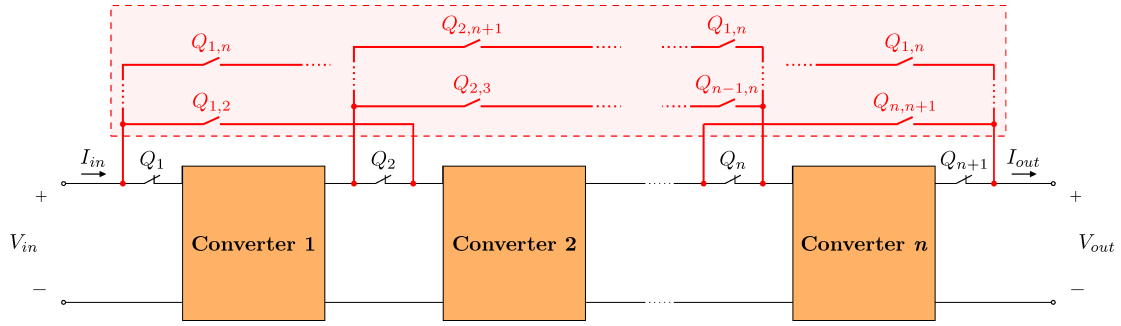


Fig. 6.5 General structure of a fault-tolerant cascaded converter [122]. Each orange block represents a simpler DC–DC converter. Bypass switches are highlighted in the light-red area.

6.1.2.2. Inclusion of discrete components

Fault-tolerant converter architectures based on additional discrete components may either employ redundant components, whose principals of operation are identical to those integrated in the original DC–DC converter; or alternative components, whose principals of operation differ from the ones used in the original DC–DC converter topology. Among other technologies, it is common to consider the adoption of MOSFETs, IGBTs, TRIACs, or auxiliary transformer windings.

The additional discrete components introduced in fault-tolerant converters do not necessarily aim to directly replace the functions of the faulty switch(es). In FB DC–DC converters, the reduction of the converter output voltage is the most relevant side effect arising from OC faults in the switches of the transformer primary-side bridge. Therefore, reconfiguration strategies suitable for FB DC–DC converters aim to compensate the decay in the output voltage. One of those fault-tolerant architectures requires an additional redundant transformer winding, placed in the transformer secondary winding [55], following the configuration shown in Fig. 6.6. The auxiliary winding is activated once a faulty switch impairs the operation of the transformer primary-side bridge.

The insertion of an auxiliary transformer winding as mean to compensate the reduction of the converter output voltage involves a fairly high implementation cost. Alternative reconfiguration strategies provide feasible and cheaper solutions to the same problem. To recover the pre-fault voltage level at the converter output, a simple boost

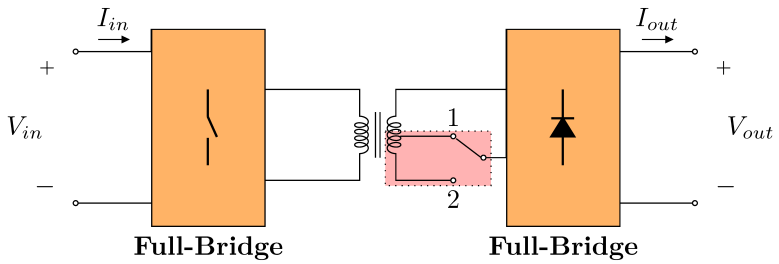


Fig. 6.6 Fault-tolerant FB DC–DC converter based on an auxiliary winding in the transformer secondary winding [55].

converter is connected, in a cascaded configuration, in either the transformer primary-side [123] or the transformer secondary-side [124]. A third alternative reconfiguration strategy also provides a solution for the voltage decay problem in FB and multilevel series-resonant DC–DC converters. Two capacitors and two power switches are added to the FB rectifier connected in the transformer secondary-side, thus obtaining a voltage doubler configuration [125]–[127].

Aiming the improvement of fundamental, well-established converter topologies, as it is the case of the non-isolated buck converter [128], the switched-capacitor DC–DC converter [129], or the inductor-inductor-capacitor (LLC) DC–DC converter [130], there are a few contributions in the literature that rely on additional discrete components to achieve fault tolerance of those topologies. For instance, a fault-tolerant buck-boost converter is derived from the rearrangement of a non-isolated buck converter, along with the inclusion of one additional switch [128].

In most multilevel DC–DC converters and, particularly, in the non-isolated three-level DC–DC converter, a single OC fault dictates the complete loss of power conversion capabilities. The fault-tolerant architecture of a non-isolated three-level DC–DC converter, depicted in Fig. 6.7, consists of a rearrangement of the converter input. One TRIAC and two additional passive components are displaced in a manner that allows to accommodate multiple voltage sources, connected in series, at the input of the multilevel converter [62]. Despite the partial loss of power conversion capability, the extension of the converter operation is ensured with this fault-tolerant architecture [62].

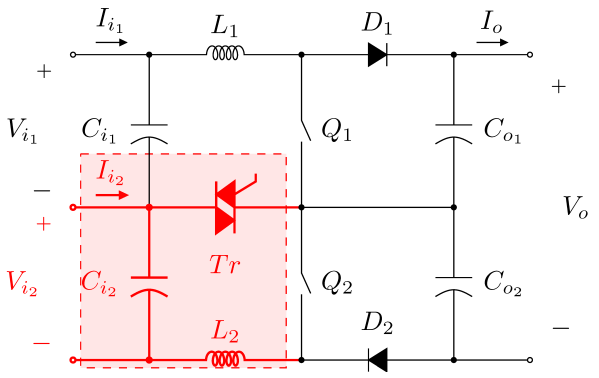


Fig. 6.7 Fault-tolerant non-isolated three-level DC–DC converter [62]. Additional components introduced in the fault-tolerant converter architecture are highlighted in red.

Due to the lack of redundancy of the single-switch buck converter, a single OC fault completely shuts down the converter operation. To solve the problem, a fault-tolerant architecture of a buck converter is derived from the equivalent circuit of two distinctive DC–DC converter topologies [131]. Operation at either buck or buck/boost mode is feasible while adopting such fault-tolerant architecture. In comparison to the traditional buck converter, the fault-tolerant buck converter includes one additional power switch [131].

In very few cases, the inclusion of discrete components aims to assist on the implementation of the fault-tolerant operation of converters whose original architecture is inherently tolerant against faults. The main objective is to achieve improved performance and/or reduce the stress imposed to the healthy components. The three-phase FB converters described in [132] fits into such category. It resorts to additional switches to fully isolate the faulty leg, thus ensuring enhanced performance over the post-fault period.

The main advantage of reconfiguration strategies based on the inclusion of discrete components lies on the simplicity of the post-fault control, which is usually quite resemblant to the pre-fault control structure. The reduced number of components required to deploy the fault-tolerant DC–DC converter architectures is also advantageous. On the other hand, potential negative side-effects associated to specific converter architectures, such as the partial loss of conversion capability or the re-arrangement of the converter input and/or output, are the main drawback usually related to such reconfiguration strategies.

6.1.2.3. Inclusion of redundant legs

Fault-tolerant architectures based on redundant legs aim to perform a direct replacement of the faulty switch(es). Such redundant leg can be used in full, i.e., all the devices of the leg are operated in the post-fault period, or used partially, i.e., only a single switching device of the leg operates in the post-fault period (the device considered more suitable to that end). Typically, a redundant leg consists of redundant switch(es) and, whenever applicable, other auxiliary components.

The fault-tolerant architecture of a single-switch DC–DC boost converter [58], [61] represents a good example of a fault-tolerant architecture based on redundant legs. The redundant leg, composed of one switch and one TRIAC [58], or just one switch [61], is placed in parallel with the original converter switch. If the original converter switch becomes faulty, the redundant leg is activated. This reconfiguration strategy only becomes an interesting and cost-effective solution when employed in more elaborated converter assemblies, composed of an association of several single-switch boost DC–DC converters [58], [61], as depicted in Fig. 6.8. In that case, a single redundant leg effectively replaces a faulty switch of any of the converters/modules.

The fault-tolerant DAB converter proposed in [133] represents a good example of a fault-tolerant DC–DC converter adopting partial utilisation of a redundant leg. Based on the position of the faulty device, the reconfiguration strategy selects the appropriate component of the leg to assure a smooth post-fault operation.

Thanks to the inclusion of redundant legs, smooth post-fault operation is secured. At the same time, very little modifications occur on the conversion capabilities and on the

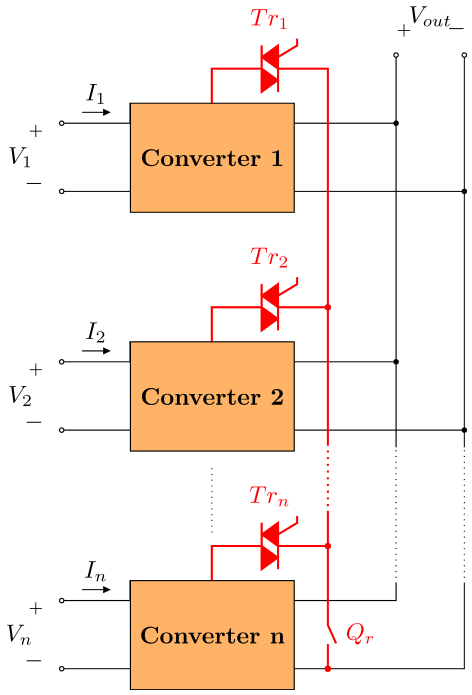


Fig. 6.8 Implementation of a redundant converter leg based on a single redundant switch (Q_r) [58], [61].

stress imposed to the healthy converter components. Such advantages come at the expense of a more complex and expensive hardware architecture.

6.2. Developed fault tolerance strategies

The evaluation made to the literature related to fault tolerance on DC–DC converters reveals the notorious lack of power conversion solutions capable of providing high reliability and availability, particularly suitable for homes and offices applications. Such observation is common to the entire range of DC–DC converter architectures. Particularly, it is obvious the lack of fault-tolerant DC–DC converters for niche and emerging applications, with relevance within the context of homes and offices, as it is the case of LED lighting.

Following sub-sections present the fault tolerance strategies developed in the framework of this work. They aim to answer to the challenges of simplicity, low implementation effort, and effectiveness.

6.2.1. General appliances

It is recalled that the DC–DC converter topology of excellence for general appliances, considered in this study, is the non-isolated unidirectional interleaved DC–DC converter.

Despite its inherent redundancy, the operation of interleaved DC–DC converters under faulty conditions has critical side-effects, especially when no reconfiguration measures are developed. The most prominent ones include:

- Increment of the ripple on the converter input and output currents;

- Poor current sharing among the healthy converter' phases;
- Additional current ripple in the output electrolytic capacitor, leading to overheating and consequent curtailment on the capacitor useful lifetime [134].

Apart the potential negative impact on the equipment being supplied by a faulty DC–DC converter, the aforementioned side-effects also have potential to further degrade the condition of the converters and eventually conduce to catastrophic failures.

Phase-shift correction is typically adopted in the reconfiguration of faulty interleaved DC–DC converters. Such action reduces, in general, the converter input current ripple after a fault. Unfortunately, it does not allow to re-establish pre-fault ripple levels. Therefore, the adoption of additional actions reveals fundamental to enhance the response of the converter, by reducing the ripple of the converter input current to pre-fault levels.

As demonstrated in [40], the switching frequency f_{sw} can be controlled in a way that minimises the ripple in the converter phase currents which, in turn, will minimise the ripple of the current at the converter input and output. Thus, a control strategy consisting of a combination of adaptive phase-shift and frequency variation can perform the reconfiguration task with good results.

6.2.1.1. Phase-shift correction

According to the information available in the controller regarding the presence and location of faulty phases, it is possible to establish the phase-shift to apply between each gating signal, over the post-fault period.

Under healthy condition, the phase-shift between gating signals is defined as:

$$\varphi = \frac{2\pi}{n} \tag{6.1}$$

where φ is the phase-shift between gating signals, given in *rad*, and n denotes the number of converter phases.

For the post-fault period, the phase-shift to be imposed between the gating signals assigned to healthy switches should be defined as:

$$\varphi' = \frac{2\pi}{m} \tag{6.2}$$

where m denotes the number of converter phases that remain functional.

6.2.1.2. Switching frequency correction

The increment of the switching frequency f_{sw} during the post-fault period aims to re-establish the frequency of the input current ripple to pre-fault levels. The switching frequency f_{sw} to impose assumes predefined discrete values and is conditioned by the converter initial switching frequency.

For an interleaved DC–DC converter, the frequency of the input current ripple $f_{I_{in}}$ is computed as:

$$f_{I_{in}} = n f_{sw} \tag{6.3}$$

where n denotes the number of converter phases and f_{sw} denotes the converter switching frequency.

In case that an OC fault impairs the operation of the converter, the frequency of the input current ripple $f'_{I_{in}}$ will decrease, and will be given by:

$$f'_{I_{in}} = m f_{sw} \tag{6.4}$$

where $f'_{I_{in}}$ refers to the frequency of the input current ripple over the post-fault period, m denotes the number of healthy converter phases and f_{sw} denotes the converter switching frequency. It is important to note that condition (6.4) is solely valid in case that the phase shift between control signals is corrected after the fault, according to the terms described in Section 6.2.1.1.

In case that no reconfiguration is adopted with regards to switching frequency, frequency $f'_{I_{in}}$ will be lower than the pre-fault one. As the amplitude of the current ripple ΔI_{in} is proportional to the frequency $f'_{I_{in}}$, the post-fault operation will have as consequence the increment of ΔI_{in}. Keeping the frequency $f'_{I_{in}}$ equal to the pre-fault value ($f_{I_{in}}$) will allow to effectively banish the increment of ΔI_{in}, even under faulty conditions.

The following condition must be met to recover the pre-fault frequency of the input current ripple ($f_{I_{in}}$):

$$f'_{sw} = \frac{n}{m} f_{sw} \tag{6.5}$$

where f'_{sw} denotes the switching frequency to be imposed during the post-fault period.

6.2.1.3. Losses analysis

It is worth noting that the implementation of the reconfiguration strategy, just like in any other converter working under faulty conditions, leads to higher current rates in the healthy power switches, that remain operational, thus imposing additional conduction and switching losses, with possible overheating.

A pretty good estimation of the switching losses P_{sw} occurring in a converter switch can be obtained using the following relation, which results from a normalisation of the conditions and parameters defined in the datasheet of the switch [135]:

$$P_{sw} = (E_{on} + E_{off}) \times \frac{V_{DC}}{V_{DC_{nom}}} \times \frac{I_{sw_{pk}}}{I_{sw_{nom}}} \times f_{sw} \tag{6.6}$$

where E_{on} denotes the energy dissipated during the turn-on period, E_{off} refers to the energy

dissipated during the turn-off period, V_{DC} denotes the measured converter input voltage, $V_{DC_{nom}}$ refers to the switch rated DC-link voltage, $I_{sw_{pk}}$ denotes the measured peak switch current, $I_{sw_{nom}}$ denotes the nominal switch current, and f_{sw} denotes the switching frequency. E_{on}, E_{off}, $V_{DC_{nom}}$, and $I_{sw_{nom}}$ are constants that are defined in the datasheet of the switch and, consequently, they do not have a direct impact on the variations of the switching losses for the post-fault period. On the other hand, the peak switch current $I'_{sw_{pk}}$ and the switching frequency f'_{sw}, both measured during the post-fault period, increase after a switch failure. In the case of the three-phase unidirectional interleaved DC–DC converter, both variables increase by 1.5 times with reference to the pre-fault values:

$$I'_{sw_{pk}} = \frac{3}{2} \times I_{sw_{pk}} \tag{6.7}$$

$$f'_{sw} = \frac{3}{2} \times f_{sw} \tag{6.8}$$

All other variables with impact on the switching losses P_{sw}, expressed in (6.6), remain unchanged for the post-fault period. Therefore, the relation between the switching losses at the post-fault period P'_{sw} and pre-fault period P_{sw} is:

$$P'_{sw} = \frac{9}{4} \times P_{sw} \tag{6.9}$$

In order to properly account the influence of the proposed reconfiguration strategy on the increment of the switching losses, the impact of the increment of the switching frequency f_{sw} in the switching losses should be evaluated independently, without considering the contribution of the peak switch current $I'_{sw_{pk}}$. As f_{sw} increases by 1.5 times during the post-fault period, with reference to the pre-fault period, it is concluded the increment of f_{sw} solely contributes by 1.5 times to the overall increment of the switching losses verified in the post-fault period.

In general, the switching losses have a minor contribution to the overall losses of the DC–DC converter, regardless of the converter operating conditions [136], [137]. Moreover, fault-tolerant operation is envisioned only for a limited period of time, until the normal converter condition can be re-established. Still, converter operation with full load conditions should be avoided during post-fault operation, given the expected additional stress imposed to the healthy converter components. Besides, f_{sw} must respect the limitations imposed by the converter components. For converters based on IGBT technology, the switching frequency f_{sw} is typically limited to 20 *kHz*.

6.2.1.4. Simulation results

To evaluate the impact of each one of the reconfiguration measures (phase-shift and switching frequency correction), three distinctive scenarios of operation have been

established:

1. As for the first scenario, no reconfiguration is adopted, meaning that the modulation of the converter control signals remains unchanged after the fault.
2. For the second scenario, partial reconfiguration is adopted, i.e., the modulation of the converter control signals is partially adapted, through the correction of the phase-shift between the gating signals assigned to healthy switches.
3. In the third scenario, full reconfiguration is considered, meaning that the modulation of the converter control signals is fully adapted, through the correction of both the switching frequency and the phase-shift between the gating signals assigned to healthy switches.

The effectiveness of the reconfiguration strategies was validated theoretically through a dedicated simulation model, developed in *Simulink™* environment. The configuration of the model, along with the adopted parameters are described with detail in Appendix A.1.

Fig. 6.9 depicts the converter input current for those three circumstances: in Fig. 6.9 (a), no reconfiguration is used after an OC failure; in Fig. 6.9 (b), only phase-shift correction is employed (partial reconfiguration); and in Fig. 6.9 (c) both phase-shift and switching frequency correction are applied (full reconfiguration).

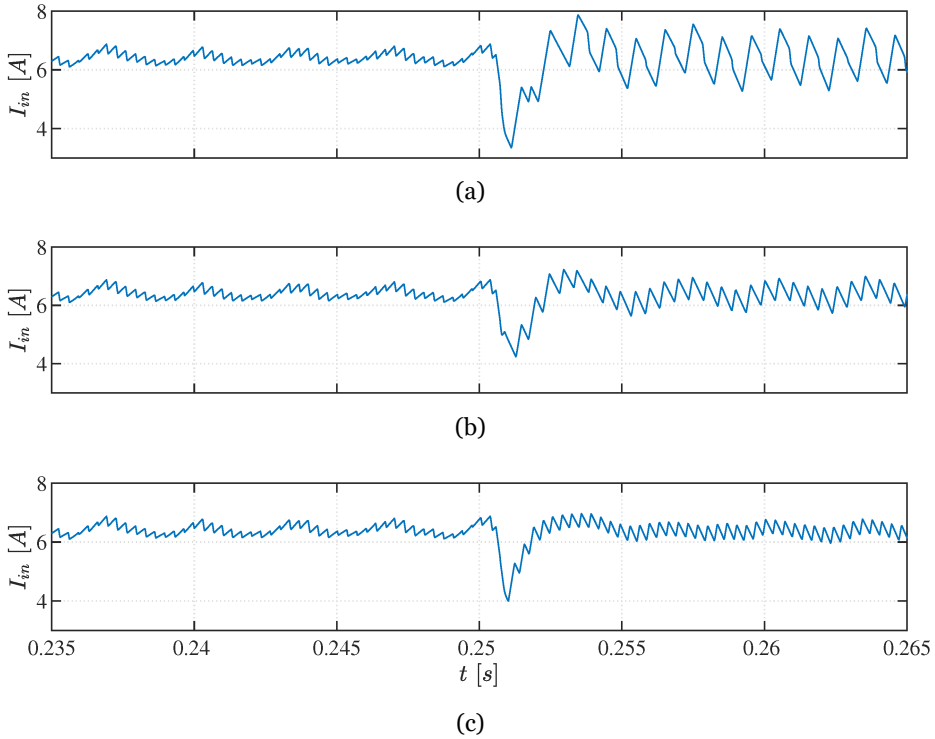


Fig. 6.9 Evolution in time of the converter input current I_{in}, observed in case of an OC fault, taking place at t = 0.25024 s. The following post-fault scenarios are considered: (a) no reconfiguration; (b) partial reconfiguration; (c) full reconfiguration. The output voltage V_{out} is 60 V and the pre-fault switching frequency f_{sw} is 1 kHz.

As demonstrated in Fig. 6.9 (a), the OC fault promotes a significant amplification on the ripple of current I_{in}, induced by the unbalanced switching pattern and the lower ripple frequency. In healthy converter operation, the ripple of I_{in} is 0.76 A. After the fault, the ripple of I_{in} increases 3 times, reaching 2.11 A. The results of Fig. 6.9 (b) and Fig. 6.9 (c) show a decrement in the ripple of I_{in}, as a result of the converter reconfiguration. Thanks to the implementation of phase-shift adjustment – refer to Fig. 6.9 (b) – the ripple of I_{in}, equal to 1.21 A, is halved with reference to the scenario of no reconfiguration. Even though phase-shift plays an important role in ripple minimisation after an OC fault – refer to Fig. 6.9 (b) – further improvements in the limitation of ripple are attained after combining the increase of f_{sw} with phase-shift correction, as depicted in Fig. 6.9 (c). The ripple of I_{in}, equal to 0.76 A during both the pre-fault and post-fault periods, is kept unchanged, thanks to the combination of phase-shift adjustment and increment of f_{sw}.

6.2.1.5. Experimental results

To validate the simulation results presented in Section 6.2.1.4, operation scenarios similar to those adopted in simulation were replicated in experimental context. The architecture and parameters of the laboratory prototype are described with detail in Appendix B.1.

Experimental data also confirm the effectiveness of the reconfiguration strategy based on the combination of phase-shift adjustment and switching frequency increment, as shown in Fig. 6.10. In Fig. 6.10 (a), no reconfiguration is applied. A significant increment in the ripple of I_{in} is observed, as one of the converter phases stopped working. Concurrently, the remaining phases are controlled resorting to an unbalanced switching pattern. When partial reconfiguration is employed – refer to Fig. 6.10 (b) – the balance of the switching pattern is re-established, resulting in a significant reduction of the I_{in} ripple. Still, slightly higher levels of ripple are verified after the fault. In case that full reconfiguration is applied – refer to Fig. 6.10 (c) – the switching pattern balance is re-established and the switching frequency f_{sw} increases from 1 kHz to 1.5 kHz. Ripple levels are further reduced, allowing to recover the level of ripple observed in the pre-fault period.

The benefits of the reconfiguration strategies go well beyond the curtailment of the I_{in} ripple. To quantify all the benefits of the reconfiguration strategies, Fig. 6.11 to Fig. 6.14 establish a comparison between the different reconfiguration scenarios. Data was collected from the experimental results and compiled in the form of four distinctive performance metrics: relative input current ripple (ΔI_{in}), output capacitor current ripple (ΔI_{Cap}), relative current unbalance between healthy converter phases (ΔI_{ph}), and power conversion efficiency (η). These performance metrics are mathematically defined using the expressions (6.10) to (6.13), and are based on data obtained along the post-fault converter

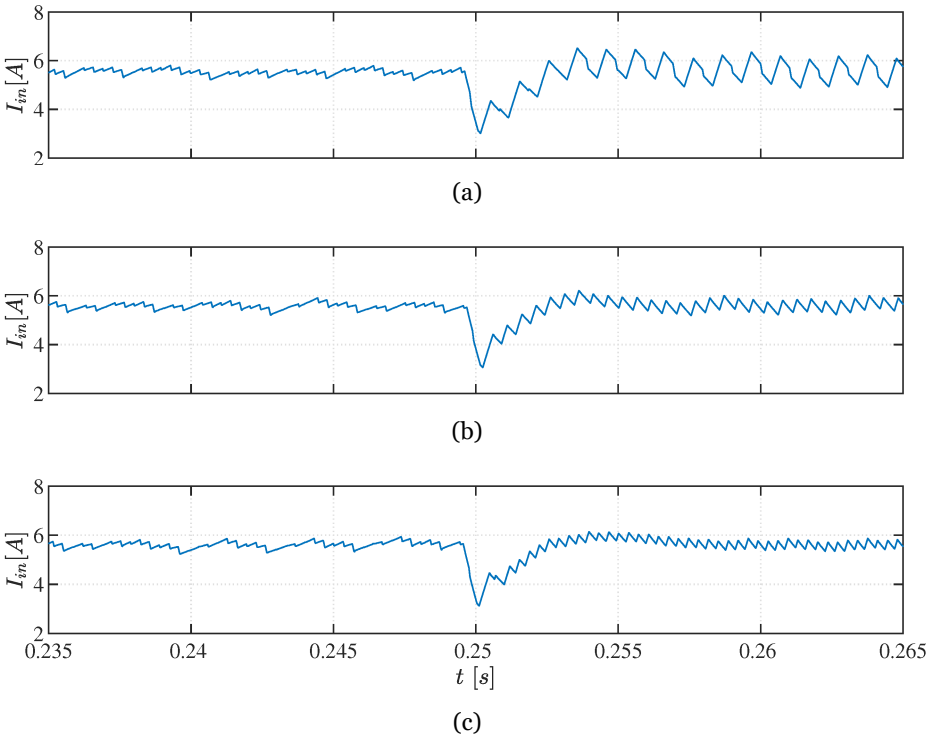


Fig. 6.10 Evolution in time of the converter input current I_{in}, observed in case of an OC fault, taking place at t = 0.2495 s. The following post-fault scenarios are considered: (a) no reconfiguration; (b) partial reconfiguration; (c) full reconfiguration. The pre-fault switching frequency f_{sw} is 1 kHz and the output voltage V_{out} is set at 60 V.

operation, when steady-state conditions are recovered:

$$\Delta I_{in} = \frac{I_{in_{\max}} - I_{in_{\min}}}{I_{in}} \times 100 \tag{6.10}$$

$$\Delta I_{Cap} = I_{Cap_{\max}} - I_{Cap_{\min}} \tag{6.11}$$

$$\Delta I_{ph} = \frac{\left| I_2 - I_3 \right|}{I_{in}} \times 100 \tag{6.12}$$

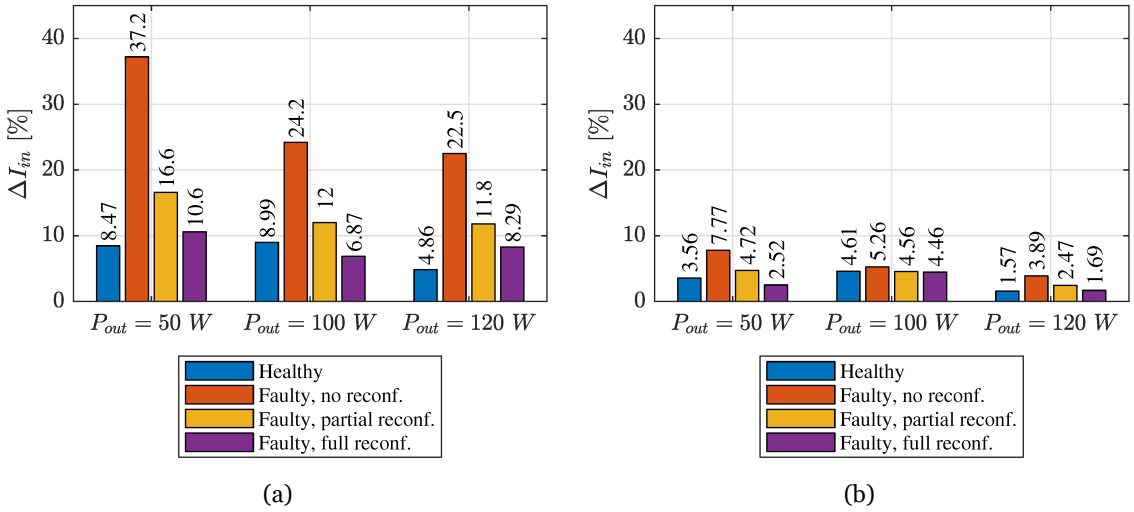
$$\eta = \frac{P_{out}}{P_{in}} \times 100 \tag{6.13}$$

A brief and global evaluation of the results provided in Fig. 6.11 to Fig. 6.14 demonstrates that the adoption of the reconfiguration strategies successfully reduce the side-effects arising from OC faults on the converter switches.

Referring to Fig. 6.11, where the relative input current ripple (ΔI_{in}) is analysed, it is noticed the remarkable impact of the reconfiguration strategies, through the attenuation of ΔI_{in} to levels observed prior to the fault. Looking at Fig. 6.11 (a), where the converter switching frequency is equal to 1 kHz, it is stated that the OC fault promotes a sharp increment of ΔI_{in}. For such scenario, ΔI_{in} increases by 4.4 times, 2.7 times, and 4.6 times, when the output power is 50 W, 100 W, and 120 W, respectively. Referring to Fig. 6.11 (b),

where the converter switching frequency is equal to 5 *kHz*, it is noted that there is a smaller yet important impact of the fault on ΔI_{in}. Under such conditions, ΔI_{in} increases by 2.2 times, 1.1 times, and 2.5 times, when the output power is 50 *W*, 100 *W*, and 120 *W*, respectively.

The evaluation of the results provided in Fig. 6.11 (a) and Fig. 6.11 (b) also reveal that the major contribution to the attenuation of ΔI_{in} derives from the application of phase-shift correction, as it is the reconfiguration strategy that enables the most significant decay on ΔI_{in}. Such trend is particularly noticeable at low switching frequency, as noted on Fig. 6.11 (a).



(a) (b)

Fig. 6.11 Evolution of the relative input current ripple according to the adopted reconfiguration strategies. The results are grouped according to the switching frequency: (a) f_{sw} = 1 *kHz*; (b) f_{sw} = 5 *kHz*.

The results provided in Fig. 6.12, concerning the ripple observed in the output capacitor current (ΔI_{Cap}), also reveal the positive impact of the reconfiguration strategies on the minimisation of ΔI_{Cap}. The impact of the fault is particularly prominent for low switching frequency, as shown in Fig. 6.12 (a). At a switching frequency of 1 *kHz*, the fault induces an increment of 2.3 times in ΔI_{Cap}, for all the three levels of output power considered in the evaluation.

As expected, the reconfiguration of the converter promotes the approximation of ΔI_{Cap} to levels observed before the fault. Once again, it is noted that the correction of phase-shift assures the most significant decay on ΔI_{Cap}. Referring to the scenario of output power equal to 120 *W*, at a switching frequency of 1 *kHz* – represented in the right-hand side of Fig. 6.12 (a) – it is stated that the correction of phase-shift contributes to 93 % of the reduction observed on ΔI_{Cap}, while the correction of the switching frequency contributes with 7 % to the reduction on ΔI_{Cap}.

Despite the very positive impact of the adoption of reconfiguration strategies on the minimisation of ΔI_{Cap}, it is not possible to fully recover the levels of ΔI_{Cap} observed prior to the fault. According to Fig. 6.12 (a), ΔI_{Cap} increases by 22 %, 32 %, and 37 %, over the pre-

fault values, after adopting full reconfiguration of the converter, when the output power is 50 *W*, 100 *W*, and 120 *W*, respectively.

As for the scenarios adopting a switching frequency of 5 *kHz* – refer to Fig. 6.12 (b) – the results reveal a fairly smaller impact of the OC fault on the variation of ΔI_{Cap}. Translating into numbers, the fault incurs an increment in ΔI_{Cap} comprised between 1.5 times and 1.6 times, for all the three levels of output power.

As a result of the converter reconfiguration, there is a small reduction on ΔI_{Cap}. By establishing a comparison between the scenarios of no reconfiguration and full reconfiguration, it is concluded that the reduction of ΔI_{Cap} reaches 0 %, 6 %, and 4 %, when the output power is 50 *W*, 100 *W*, and 120 *W*, respectively. It is interesting to note that the results of Fig. 6.12 (b) reveal the increment of the switching frequency as the most effective measure to recover ΔI_{Cap}. It is also shown that the reconfiguration strategies do not allow to fully recover the levels of ΔI_{Cap} observed prior to the fault. According to Fig. 6.12 (b), ΔI_{Cap} increases by 47 %, 39 %, and 55 %, over the pre-fault values, after adopting full reconfiguration of the converter, when the output power is 50 *W*, 100 *W*, and 120 *W*, respectively.

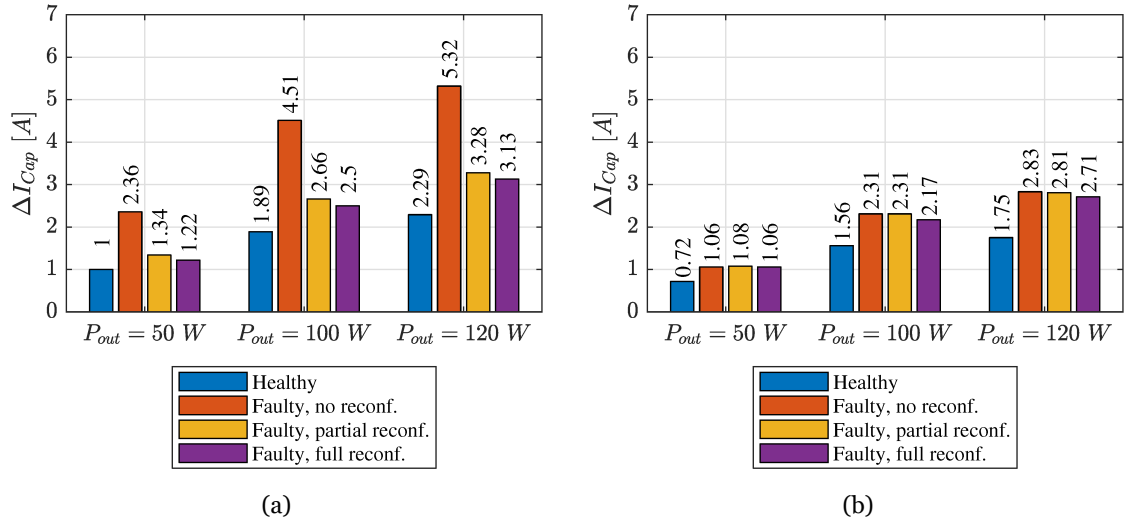
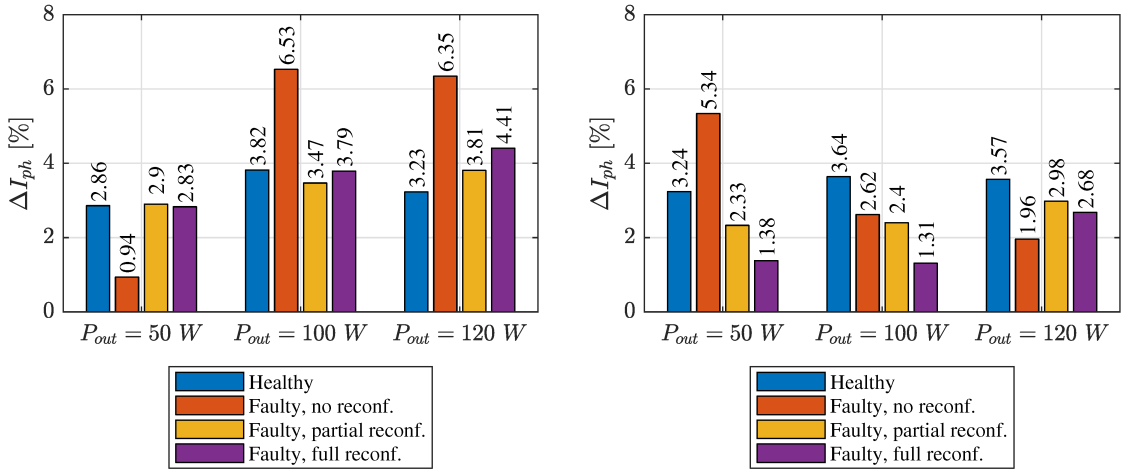


Fig. 6.12 Evolution of the output capacitor current ripple as a function of the adopted reconfiguration strategies. The results are grouped according to the switching frequency: (a) f_{sw} = 1 *kHz*; (b) f_{sw} = 5 *kHz*.

Keeping the relative current unbalance (ΔI_{ph}) as low as possible is a critical aspect in the sense of extending the lifetime of the converter and, at the same time, ensuring its proper operation. Fig. 6.13 shows the relative current unbalance (ΔI_{ph}) observed for the reconfiguration scenarios considered in the evaluation. It is not possible to establish a uniform and distinctive pattern of evolution. In other words, there are scenarios in which the fault condition degrades the unbalance between phase currents, as for instance the scenario P_{out} = 120 *W*, at f_{sw} = 1 *kHz*; in other scenarios, the fault condition has very little

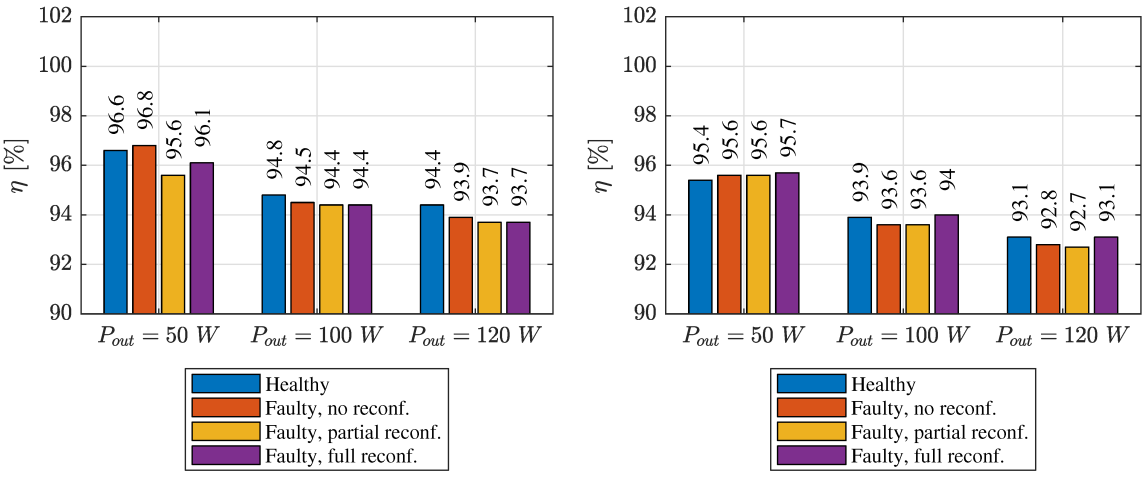
impact or even decreases the unbalance between phase currents, as it is observed for scenario P_{out} = 50 W, at f_{sw} = 1 kHz and scenario P_{out} = 120 W, at f_{sw} = 5 kHz. Regardless of that, the most important goal is attained in all scenarios, i.e., the deployment of the reconfiguration strategies assures the minimisation of the unbalance between phase currents.



(a) (b)

Fig. 6.13 Evolution of the relative current unbalance between healthy converter phases as a function of the adopted reconfiguration strategies. The results are grouped according to the switching frequency: (a) f_{sw} = 1 kHz; (b) f_{sw} = 5 kHz.

Fig. 6.14 provides the results related to the conversion efficiency (η), measured for each reconfiguration condition. Overall, neither the OC fault nor the adoption of reconfiguration strategies introduce major modifications on the levels of η. A closer look over the scenarios adopting a switching frequency of 1 kHz – represented in Fig. 6.14 (a) – shows a progressive yet minor decay on η as the complexity of the reconfiguration increases.



(a) (b)

Fig. 6.14 Evolution of the converter efficiency as a function of the adopted reconfiguration strategies. The results are grouped according to the switching frequency: (a) f_{sw} = 1 kHz; (b) f_{sw} = 5 kHz.

Such behaviour can be explained, in part, by the higher switching losses inherent to the proposed reconfiguration strategies. The impact of the higher switching losses banishes in case that the pre-fault switching frequency is sufficiently high, as demonstrated in Fig. 6.14 (b).

In conclusion, the four performance metrics confirm the effectiveness of the reconfiguration strategies, allowing to greatly recover the power conversion capabilities of the faulty converter, without compromising aspects like reliability of the converter or the conversion efficiency.

6.2.2. LED lighting

Despite the maturity of the existing power electronics technologies used to drive LED lighting systems, there is a huge gap between the expected lifetime of power electronics and LEDs [138]. Electrolytic capacitors and active semiconductors are unable to compete with LEDs when it comes to lifetime. In practice, this means that there is a meaningful risk that the semiconductors or capacitors of the LED driver fail *a priori* to the LED device itself. Faults in either the LED driver or LED itself seriously compromise the quality of light produced, thus reducing the inhabitants' comfort.

Some solutions available in the literature successfully improve the reliability of LED drivers by reducing the required capacitance, thus allowing to replace electrolytic capacitors by alternative and more reliable capacitor technologies [24]–[26], [139], [140]. For those solutions, the threat of semiconductor faults remains a limiting factor in the lifetime of LED drivers.

In the current framework, fault tolerance on LED drivers ascertains itself as the solution of excellence to minimise the gap between the lifetime of power semiconductors and LED devices. The scientific literature provides very few contributions with regards to fault-tolerant LED drivers. The few fault-tolerant LED lighting solutions available in the literature until very recently are mostly based on linear or passive regulators [141], [142], whose efficiency is pretty limited.

Apart the extended exploitation of the LED devices' useful lifetime, simplicity, low cost, and precise dimming capability are deemed fundamental for any LED driver employed in residential lighting systems. The fault-tolerant SIMO LED driver, first introduced in [143], successfully accomplishes the aforementioned goals. Thanks to its architecture, it becomes possible to continue supplying all LED strings connected to the driver, in the event of OC faults on the semiconductors with current control functions. Even so, if no reconfiguration measures are taken in order to adapt the operation of the entire LED lighting system along the post-fault period, there is a degradation of the luminous flux

delivered by the LED string(s) connected to the faulty channel(s), due to the loss of the current control function on that channel(s).

It was previously shown, in Section 4.2.1, that a single OC fault, in any of the semiconductors with current control functions, can severely affect the average inductor current and, consequently, the amount of current delivered to each LED string. The adoption of proper software reconfiguration strategies allows to continue supplying all the LED strings and even maintain the pre-fault luminous flux in all strings. These interesting features can be easily magnified in case that multiple strings are connected to the same LED driver.

Following sub-sections introduce three distinctive approaches suitable for ensuring optimised operation of the fault-tolerant SIMO converter in the event of OC faults.

6.2.2.1. Manual dimming ratio and maximum string current correction

The luminous flux of a LED string, denoted as LED string n, directly depends on the average current $\bar{I}_n$ flowing through it. In turn, the average current $\bar{I}_n$ is a function of the dimming ratio d_{dim_n} and maximum string current I_{max_n}:

$$\bar{I}_n = d_{\mathrm{dim}_n} I_{\mathrm{max}_n} = d_{\mathrm{dim}_n} I_n . \tag{6.14}$$

Over the post-fault period, it is of interest to accurately control the average current $\bar{I}_n$, by increasing it to the pre-fault level. Based on (6.14), $\bar{I}_n$ can be either manipulated through the dimming ratio d_{dim_n} or the maximum string current I_{max_n}. Hence, two distinctive reconfiguration approaches can be selected to obtain improved response from the LED driver in post-fault operation. Both aim to re-establish the pre-fault levels of average current $\bar{I}_n$, flowing through the LED strings.

One of the approaches – denoted as reconfiguration strategy 1) – consists of adapting the dimming ratio d_{dim_n} of each LED string, taking advantage of the availability of the driver dimming switches. Sustaining the average current $\bar{I}_n$ of each LED string, through the adaption of the dimming ratio d_{dim_n}, becomes possible thanks to the ability of the fault-tolerant SIMO LED driver to attain full dimming range.

The second approach – denoted as reconfiguration strategy 2) – consists of concurrently adapting the dimming ratio d_{dim_n} and the maximum string current I_{max_n}. Since the application of the reconfiguration strategy 1) commonly results in an increment of the dimming ratio d_{dim_n}, the second approach is particularly well suited when the LED driver operates in a region with a small margin of increment of the dimming ratio d_{dim_n}. This reconfiguration measure typically implies a minor increment of the maximum current flowing in all the LED strings. For that reason, the implementation of this approach should take into account the peak forward current of the LED devices.

Table 6.1 provides a general description on how the reconfiguration strategies adapt the dimming ratio d_{dim_n} and the maximum string current I_{max_n}, during the post-fault period.

TABLE 6.1 EFFECTS OF THE IMPLEMENTATION OF THE RECONFIGURATION STRATEGIES

Reconfiguration Strategy	d_{dim_n}	I_{max_n}
reconfiguration strategy 1)	↗	=
reconfiguration strategy 2)	↗	↗

6.2.2.1.1. Simulation results

The effectiveness of the reconfiguration strategies was validated theoretically resorting to a dedicated simulation model, developed in *Simulink*™ environment. The adopted LED driver consists of a 2-channel fault-tolerant SIMO LED driver. The configuration of the model, along with the adopted parameters are described with detail in Appendix A.2.

The LED driver is operated at healthy condition, as well as faulty condition, through the emulation of OC faults in the switches with current control functions – switches S_1 and S_2 of the circuit represented in Fig. 3.5. To observe and compare the effectiveness of each reconfiguration strategy, three distinctive scenarios are defined for the LED driver' post-fault operation: a) no reconfiguration is adopted; b) reconfiguration strategy 1) is implemented; c) reconfiguration strategy 2) is implemented. Table 6.2 reports the conditions of implementation of each reconfiguration scenario.

TABLE 6.2 PARAMETERS ADOPTED FOR EACH RECONFIGURATION SCENARIO

Parameter	Pre-fault	Post-fault, no reconf.	Post-fault, reconf. 1)	Post-fault, reconf. 2)
$I_{\mathrm{max}_n}[A]$	0.15	0.15	0.15	0.2
d_{dim_1}	0.7	0.7	0.7	0.55
d_{dim_2}	0.7	0.7	0.9	0.9

Fig. 6.15 depicts the instantaneous string currents, observed before and after an OC fault in switch S_2, taking place at t = 0.25 s. Results are provided for the three distinctive scenarios of post-fault operation.

The results provided in Fig. 6.15 show that the OC fault at switch S_2 does not introduce perturbations on the waveform of current I_1. A brief analysis to the results shown in Fig. 6.15 (a) reveals that accurate current control capability is lost at LED string 2, resulting in a relevant depreciation of current I_2. As shown in Fig. 6.15 (b), the implementation of the reconfiguration strategy 1) results in a noticeable increment of the dimming ratio applied to current I_2. In turn, the implementation of the reconfiguration strategy 2) produces effects not only on current I_2, but also on current I_1, as demonstrated in Fig. 6.15 (c). The increment of the maximum current occurs at LED string 1 and, into a lesser extent, at LED string 2.

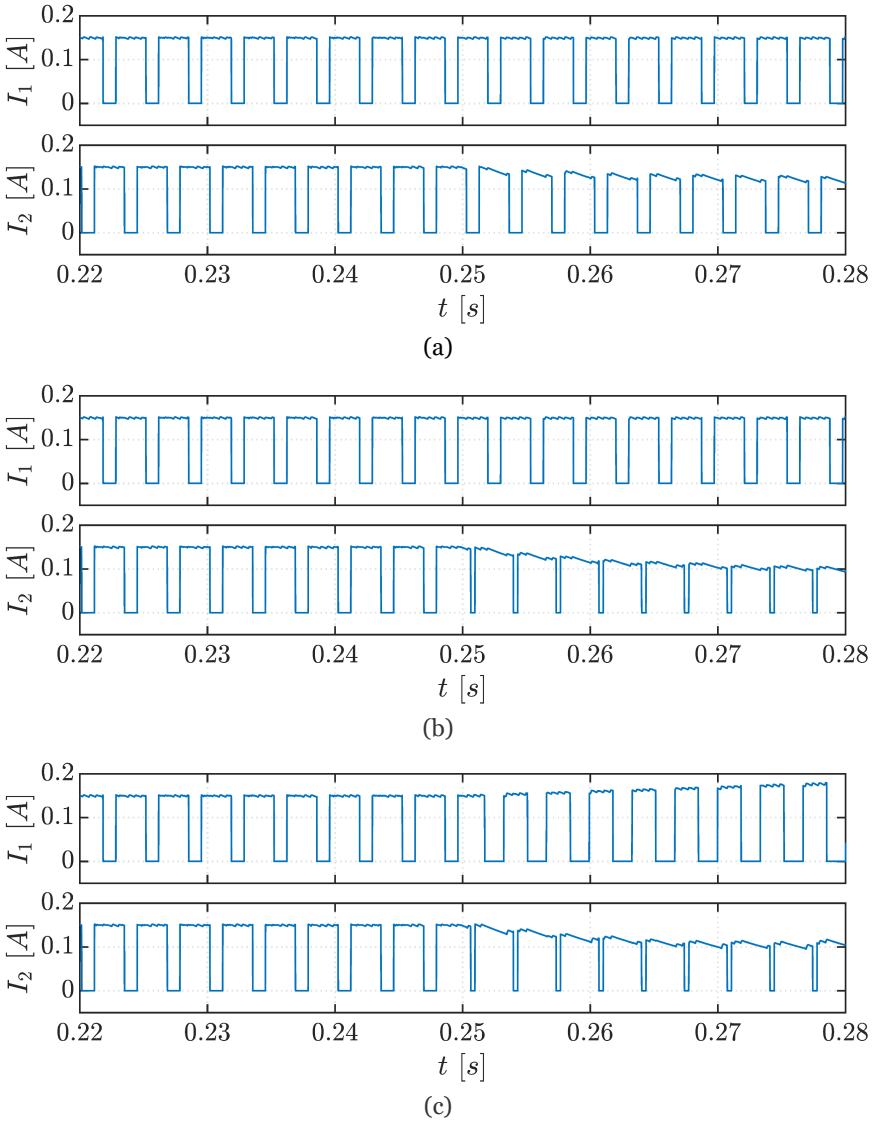


Fig. 6.15 LED strings' instantaneous currents I_1 and I_2, observed at the following operation scenarios: (a) no reconfiguration; (b) adoption of reconfiguration strategy 1) – dimming correction; (c) adoption of reconfiguration strategy 2) – dimming + max. string current correction.

To understand the effective impact of the proposed reconfiguration strategies on the luminous flux delivered by each LED string, it is important to observe the variation of the average string currents $\bar{I}_1$ and $\bar{I}_2$, after the OC fault. Fig. 6.16 shows the evolution in time of the average string currents $\bar{I}_1$ and $\bar{I}_2$, for the operation conditions considered in Fig. 6.15.

As expected, the OC fault at switch S_2 does not perturb the average string current $\bar{I}_1$ – refer to Fig. 6.16 (a) and Fig. 6.16 (b). The exception to this statement is observed at Fig. 6.16 (c), where a residual increment of current $\bar{I}_1$ takes place, as a result of the increment of $I_{\max_n}$, related to the implementation of the reconfiguration strategy 2).

With regards to the average string current $\bar{I}_2$, very distinctive patterns are observed during the post-fault operation, depending on the developed reconfiguration measures. If

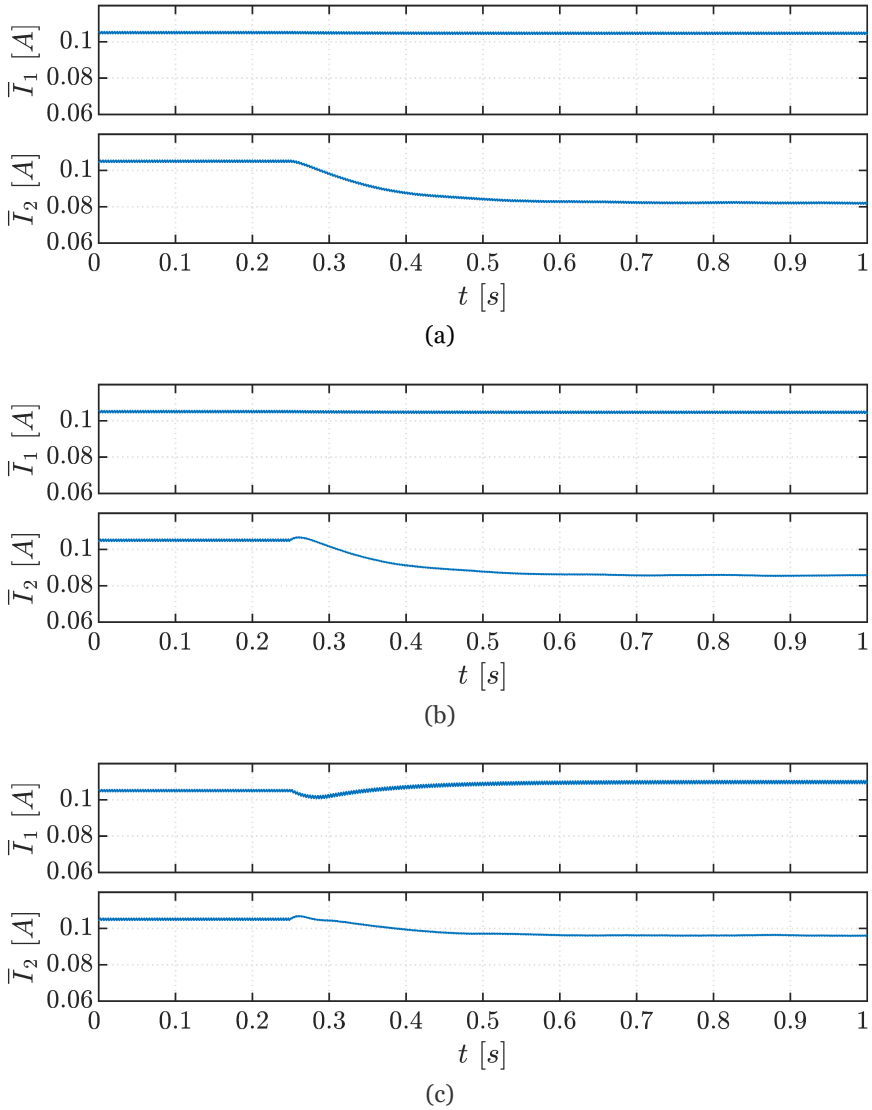


Fig. 6.16 LED strings' average currents $\bar{I}_1$ and $\bar{I}_2$, observed at the following operation scenarios: (a) no reconfiguration; (b) adoption of reconfiguration strategy 1) – dimming correction; (c) adoption of reconfiguration strategy 2) – dimming + max. string current correction.

no reconfiguration measures are deployed – refer to Fig. 6.16 (a) – the depreciation of current $\bar{I}_2$ exceeds 20 % of the pre-fault average current. The implementation of reconfiguration strategy 1) – refer to Fig. 6.16 (b) – allows for a small yet important recovery of current $\bar{I}_2$. Finally, the implementation of reconfiguration strategy 2) – refer to Fig. 6.16 (c) – allows to greatly shorten the depreciation of current $\bar{I}_2$, thanks to combined correction of dimming ratio and maximum string current.

To assess into what extent the distinctive reconfiguration measures are effective on recovering the pre-fault levels of current $\bar{I}_2$, a variable $\Delta\bar{I}_2$ is established. It provides a metric of increment of current $\bar{I}_2$, resulting from the implementation of the proposed reconfiguration strategies. Such variable is mathematically defined as follows:

$$\Delta\bar{I}_2 = \left| \frac{\bar{I}_2\left(\text{post-fault, reconf.}\right) - \bar{I}_2\left(\text{post-fault, no reconf.}\right)}{\bar{I}_2\left(\text{pre-fault}\right)} \right| \times 100. \qquad (6.15)$$

Table 6.3 summarises the results obtained for the three distinctive simulated scenarios. The average string currents $\bar{I}_1$ and $\bar{I}_2$, measured after recovering the steady-state condition over the post-fault period, are provided. Information about variable $\Delta\bar{I}_2$ is also provided.

TABLE 6.3 STRING CURRENTS IN THE PRE-FAULT AND POST-FAULT PERIODS

	No reconf.		**Reconf. strategy 1)**		**Reconf. strategy 2)**	
Parameter	Pre-fault	Post-fault	Pre-fault	Post-fault	Pre-fault	Post-fault
$\bar{I}_1$ [A]	0.105	0.105	0.105	0.105	0.105	0.11
$\bar{I}_2$ [A]	0.105	0.082	0.105	0.086	0.105	0.096
$\Delta\bar{I}_2$ [%]	–	–	–	+ 3.81	–	+ 13.3

Based on the data from Table 6.3, it is shown that the adoption of the reconfiguration strategies has potential to reduce by up to 60 % the depreciation of $\bar{I}_2$.

One of the most important features of a LED driver is precisely its ability of attaining highly accurate current control. It is important that the LED driver sustains, or at least approaches to the reference current defined for each LED string, under both healthy and faulty conditions. To assess the accuracy of the proposed fault-tolerant LED driver, the deviation of the average string current from its reference value, denoted as $\varepsilon\left(\bar{I}_n\right)$, is computed:

$$\varepsilon\left(\bar{I}_n\right) = \left| \frac{\left(d_{\dim_n} I_{\max_n}\right) - \bar{I}_n}{d_{\dim_n} I_{\max_n}} \right| \times 100. \qquad (6.16)$$

The results of the application of (6.16) are compiled in Table 6.4.

TABLE 6.4 RELATIVE DEVIATION OF THE AVERAGE STRING CURRENTS FROM THEIR REFERENCE VALUES

	Healthy	**Faulty, no reconf.**	**Faulty, reconf. strategy 1)**	**Faulty, reconf. strategy 2)**
$\varepsilon\left(\bar{I}_1\right)$ [%]	0	0	0	4.76
$\varepsilon\left(\bar{I}_2\right)$ [%]	0	21.9	18.1	8.57

These results are in line with the ones presented at Fig. 6.15, Fig. 6.16, and Table 6.4. An unacceptable deviation of the average LED string current from its reference value, verified under faulty operation and no reconfiguration, is progressively corrected and attenuated, thanks to the adoption of increasingly ammeliorated reconfiguration strategies.

6.2.2.1.2. Experimental results

Experimental tests were developed to confirm the effectiveness of the proposed LED driver and corresponding reconfiguration strategies. All the parameters of the converter components are the same as those used in simulation. The architecture and parameters of the adopted laboratory prototype are described with detail in Appendix B.2.

Just like in simulation, three distinctive scenarios are defined for the LED driver post-fault operation: a) no reconfiguration is adopted; b) reconfiguration strategy 1) is implemented; c) reconfiguration strategy 2) is implemented. An OC fault is also introduced in switch S_2, at $t = 0.25\ s$. The conditions of implementation of each reconfiguration scenario are reported in Table 6.2. Fig. 6.17 depicts the waveforms of the LED strings' currents, for the three scenarios under analysis.

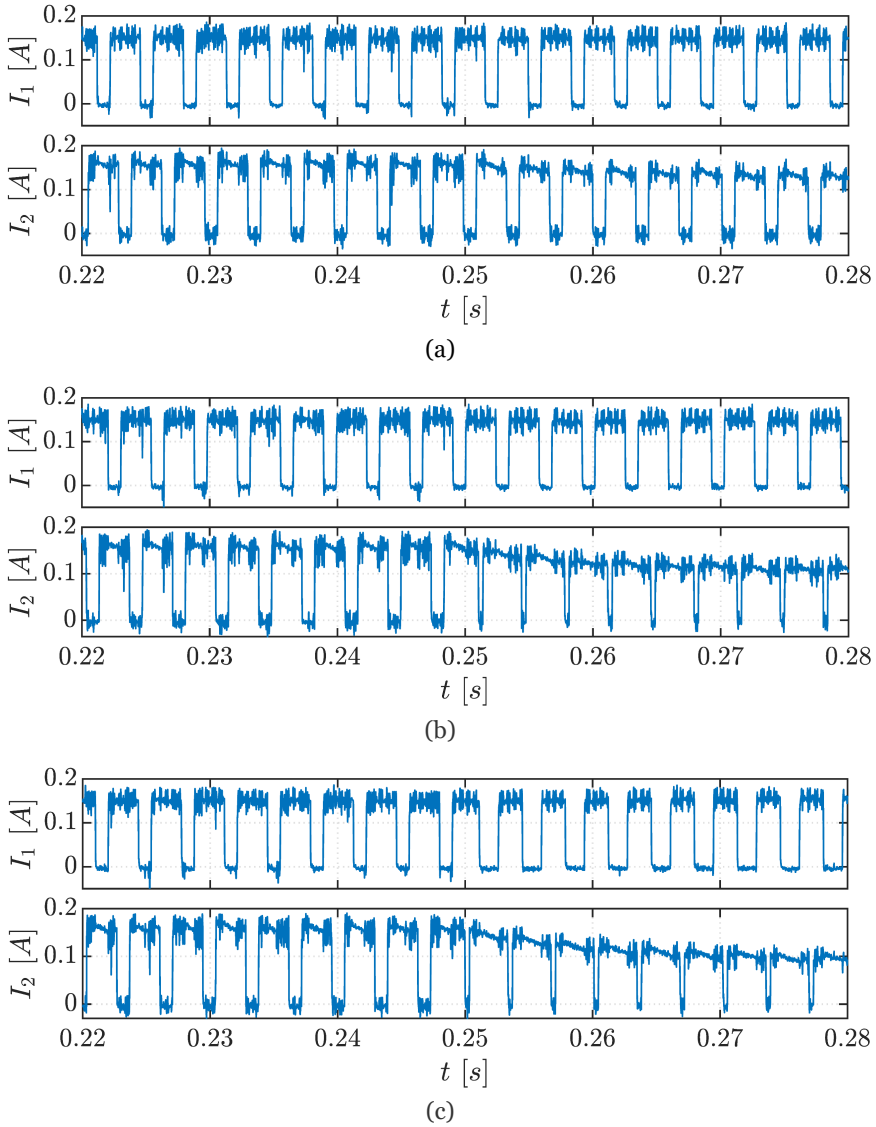


Fig. 6.17 LED strings' instantaneous currents I_1 and I_2, observed at the following operation scenarios: (a) no reconfiguration; (b) adoption of reconfiguration strategy 1) – dimming correction; (c) adoption of reconfiguration strategy 2) – dimming + max. string current correction.

The experimental results shown in Fig. 6.17 confirm the effectiveness of the converter architecture and the developed reconfiguration strategies, adopted over the post-fault converter operation. Along with the ability of the proposed converter to sustain the operation of both LED strings, the reconfiguration strategies provide relevant improvements in terms of luminous flux. Apart the presence of low-amplitude, high-frequency noise, not noticed on the simulation results, there is a good agreement between the experimental results obtained for the LED strings' instantaneous currents I_1 and I_2, and the corresponding simulation results, provided in Fig. 6.15. The high-frequency noise mainly finds its roots on the multiple switching mechanisms occurring in the LED driver: the low-frequency dimming, the medium-frequency time-sharing modulation, and the high-frequency switching responsible for the current control. Given the multi-output architecture of the converter, cross-regulation is another phenomenon playing an important role on the total harmonic distortion (THD) of the LED strings' currents.

To confirm the source(s) of the high-frequency noise, a spectral analysis is developed. Fig. 6.18 depicts the spectrum of the LED string currents, assessed in case of healthy converter operation.

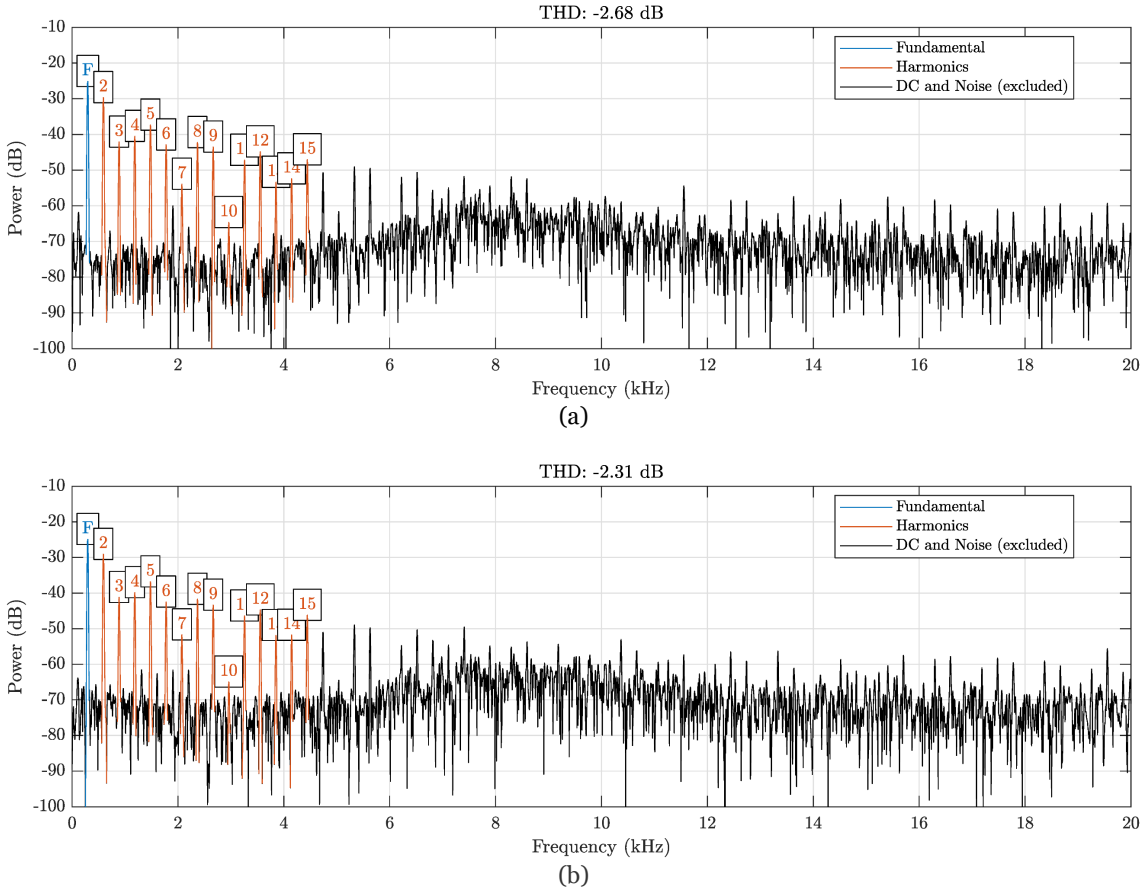


Fig. 6.18 THD of the LED strings' instantaneous currents, assessed under healthy converter operation: (a) THD_{I_1}; (b) THD_{I_2}.

The fundamental harmonic, denoted as 'F' in Fig. 6.18, is related to the dimming function and is observed at around f = 300 *Hz*. Apart the fundamental harmonic, the computation of the THD includes up to the 15th-order harmonic – corresponding to 4.5 *kHz*. As the converter operates under healthy condition, the THD of both currents is identical (-2.68 *dB* for I_1 and -2.31 *dB* for I_2).

Fig. 6.19 depicts the THD of the LED string currents, assessed in case of faulty converter operation, without implementation of any reconfiguration strategies.

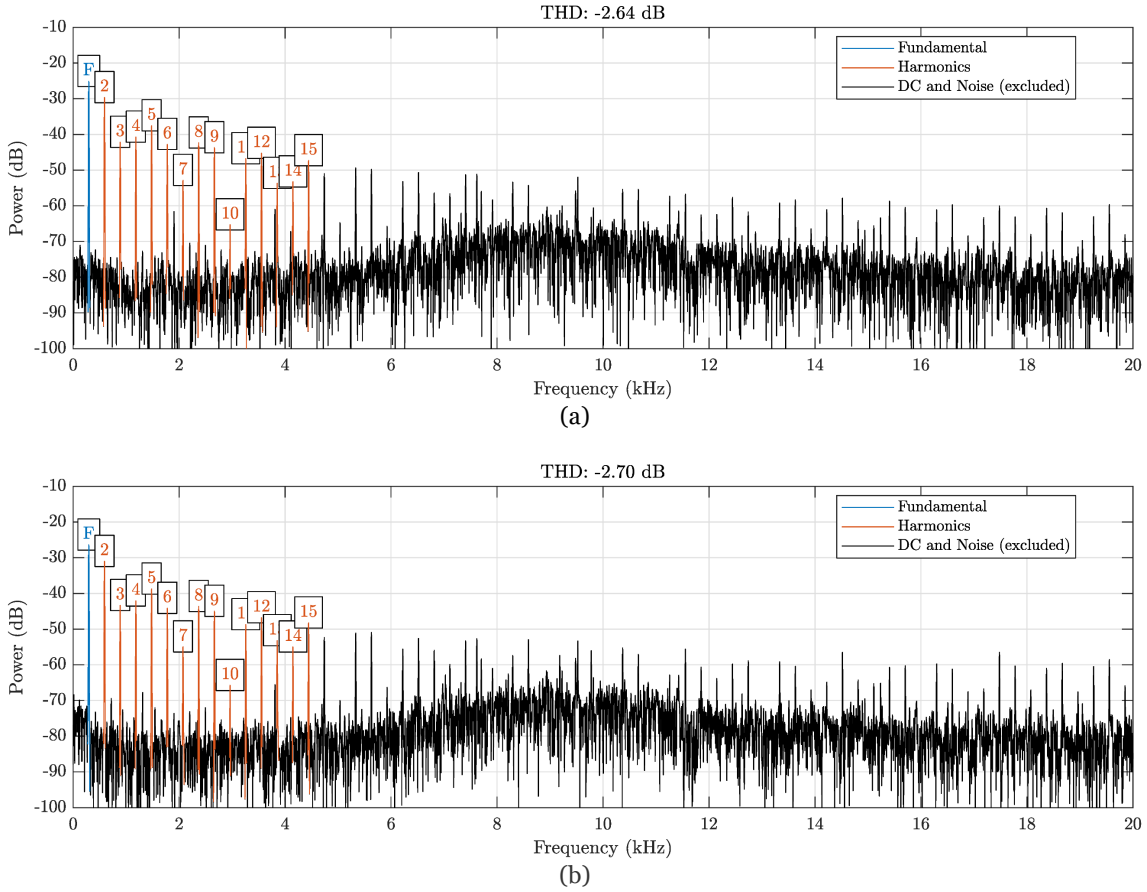


Fig. 6.19 THD of the LED strings' instantaneous currents, assessed under faulty converter operation, without implementation of reconfiguration strategies: (a) THD_{I_1}; (b) THD_{I_2}.

Based on Fig. 6.19 (b), the OC fault reduces THD_{I_2} to -2.70 *dB*. In fact, such trend is explained by the elimination of one of the switching elements from the circuit (switch S_2). Despite the reduction of the magnitude of the harmonics related to switching elements, such harmonics prevail. It is a consequence of the cross-regulation and of the dependence between the multiple outputs of the converter.

As stated in Section 6.2.2.1.1, the OC faults have an effective impact on the luminous flux delivered by each LED string, translated into the variation of the average string currents $\bar{I}_1$ and $\bar{I}_2$. Fig. 6.20 shows the evolution, in the time domain, of the average string currents $\bar{I}_1$ and $\bar{I}_2$, for the operation conditions depicted in Fig. 6.17.

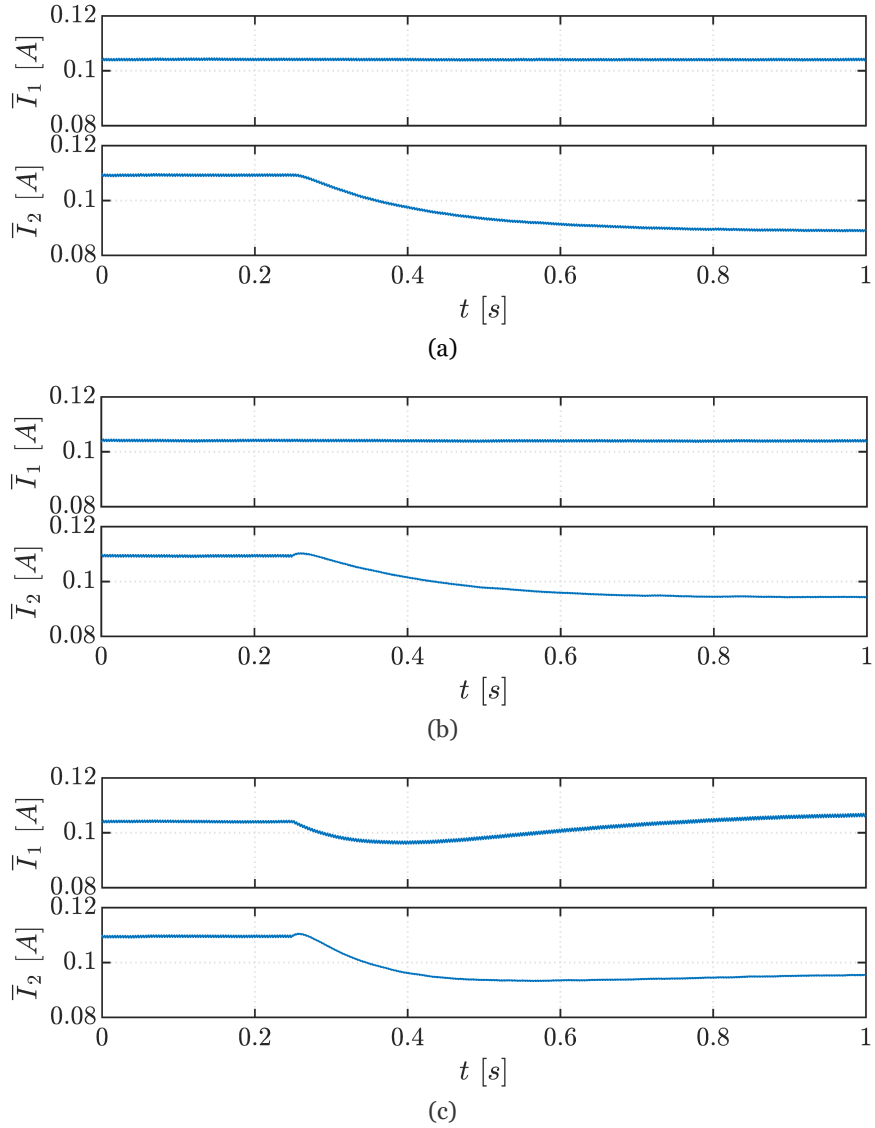


Fig. 6.20 LED strings' average currents $\bar{I}_1$ and $\bar{I}_2$, observed at the following operation scenarios: (a) no reconfiguration; (b) adoption of the reconfiguration strategy 1) – dimming correction; (c) adoption of the reconfiguration strategy 2) – dimming + max. string current correction.

Again, the results shown in Fig. 6.20 reveal a significant degree of correspondence between simulation and the experimental tests. Thanks to the reconfiguration of the converter, it is possible to greatly recover from the depreciation of luminous flux occurring because of the OC fault on switch S_2. Still, Fig. 6.20 (c) shows that the adoption of the reconfiguration strategy 2) retains a slightly smaller potential to minimise the depreciation of current $\bar{I}_2$, in comparison to the corresponding operation scenario established in simulation environment – refer to Fig. 6.16.

Table 6.5 compiles information on the average LED strings' currents $\bar{I}_1$ and $\bar{I}_2$, measured before and after introducing the OC fault at switch S_2.

TABLE 6.5 MEASURED STRING CURRENTS IN THE PRE-FAULT AND POST-FAULT PERIODS

	No reconf.		Reconf. strategy 1)		Reconf. strategy 2)	
Parameter	Pre-fault	Post-fault	Pre-fault	Post-fault	Pre-fault	Post-fault
$\bar{I}_1$ [A]	0.104	0.104	0.104	0.104	0.104	0.106
$\bar{I}_2$ [A]	0.109	0.089	0.109	0.094	0.109	0.095
$\Delta\bar{I}_2$ [%]	–	–	–	+ 4.59	–	+ 5.50

The results of Table 6.5 show that there is a residual unbalance between the average string currents $\bar{I}_1$ and $\bar{I}_2$, noticed in the healthy operation conditions. Moreover, it is shown that the adoption of the reconfiguration strategies allows to recover about 5 % of the average current flowing through String 2 (the LED string connected to the faulty converter channel). In other words, the depreciation of $\bar{I}_2$ is reduced by up to 30 %.

The application of (6.16) to the experimental data leads to the results compiled in Table 6.6.

TABLE 6.6 RELATIVE DEVIATION OF THE AVERAGE STRING CURRENTS FROM THEIR REFERENCE VALUES

	Healthy	**Faulty, no reconf.**	**Faulty, reconf. strategy 1)**	**Faulty, reconf. strategy 2)**
$\varepsilon(\bar{I}_1)$[%]	0.95	0.95	0.95	0.96
$\varepsilon(\bar{I}_2)$[%]	3.81	15.24	10.48	9.52

Just as in simulation, the significant deviation $\varepsilon(\bar{I}_2)$, introduced by the OC fault at switch S_2, is progressively attenuated, thanks to the adoption of reconfiguration measures.

6.2.2.2. Automatic dimming ratio and maximum string current correction

Despite their enormous interest and particular benefits, centralised LED driving systems like the fault-tolerant SIMO LED driver also present multiple technical challenges. Parasitic inductances and resistances associated to long cables seriously limit the luminous flux delivered by LED lighting systems that employ PWM dimming. Current compensators based on switched capacitors [29] or passive circuits [144] allow to partially recover the average current in the LEDs. Still, those solutions present important weaknesses. Additional hardware is required for the implementation of these solutions. In the case of multiple-output LED drivers, the current compensator must be replicated for each output, greatly increasing the total cost of implementation of the solution. On the other hand, hardware-based current compensators do not allow to fully recover the desired average current [29], [144].

Current compensation is also a desirable feature in order to attain the post-fault operation of fault-tolerant LED driver topologies, as set out by the strategies described in [145], [146]. Even though such reconfiguration strategies enable partial recovery of the average current flowing through the LED string(s) connected to faulty converter channels,

it is observed that manual correction of the dimming ratio and maximum string current does not allow to fully recover the desired average current.

Such limitation can be effectively overcome through the adoption of two distinctive improvements. On the one hand, a careful relocation of the timeslots which were originally assigned to the faulty semiconductor during the pre-fault period allows full exploitation of the empty timeslots and, consequently, improve the power conversion capability. On the other hand, automatic dimming and current correction facilitates tuning and selection of the dimming and maximum string current over the post-fault period. Apart the improvements made to the post-fault reconfiguration of fault-tolerant SIMO LED drivers, automatic current correction promotes resilience against variations of critical parameters of the circuit, like the cable parasitic inductance and resistance [147].

Following paragraphs introduce an analytical evaluation of the principles of operation of the fault-tolerant SIMO LED driver, now including the cable parasitic components resulting from long cabling. The structure of the converter is depicted in Fig. 6.21.

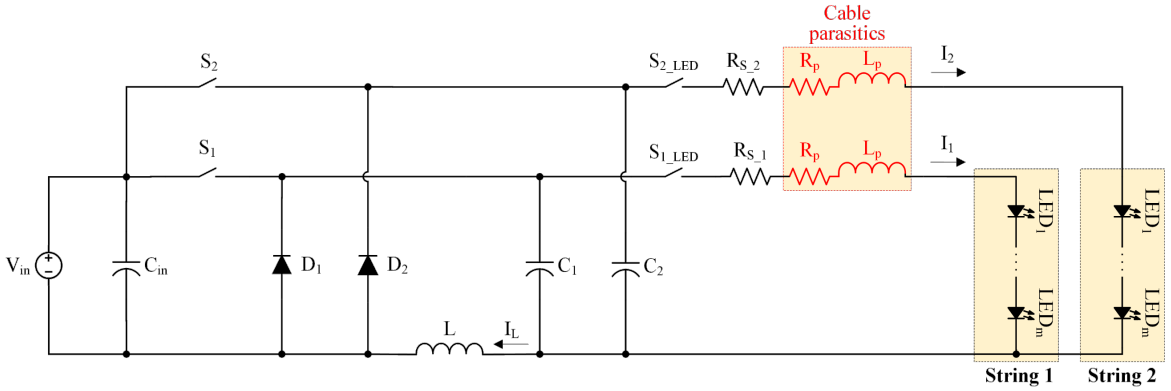


Fig. 6.21 Fault-tolerant SIMO LED driver, including the cable parasitic components resulting from long cabling.

The evaluation of the LED driver operation under both healthy and degraded modes has been previously described in the literature. Still, that evaluation does not account for the parasitic components intrinsically correlated to the long cabling.

For the analytical evaluation, each LED device is modelled as a series association of one diode, one resistor and one DC voltage source, as depicted in Fig. 2.1.

In case that the parasitics resulting from the long cabling are neglected, the average LED string current $\bar{I}_n$ is computed as:

$$\bar{I}_n = \frac{V_{in} d(t_n) - mV_E}{mR_{LED} + R_{S_n}}, n = 1,2 \qquad (6.17)$$

where V_{in} refers to the input voltage, $d(t_n)$ denotes the duty ratio observed for the timeslot t_n, V_E refers to the forward voltage drop of each LED, R_{LED} denotes the equivalent resistance of each LED device, and R_{S_n} specifies the resistance of the current sensing resistor. As the

duty ratio must be evaluated, independently, for each timeslot, the following formula should be considered for the 2-channel LED driver:

$$d(t_n) = \frac{t_{on}}{T_t}, n = 1,2 \tag{6.18}$$

where T_t denotes the period of the time-sharing carrier signal and t_{on} refers to the on-time measured during the period n.

In turn, when considering the parasitic components introduced in the circuit by the long cabling, the average string current $\overline{I}_n^*$ is given by:

$$\overline{I}_n^* = \frac{V_{in} d(t_n) - mV_E - L_p \frac{dI_n}{dt}}{mR_{LED} + R_{S_n} + R_p}, n = 1,2 \tag{6.19}$$

where L_p refers to the parasitic cable inductance and R_p denotes the parasitic cable resistance.

If equations (6.17) and (6.19) are combined and a ratio between them is established, the following expression is obtained:

$$\frac{\overline{I}_n^*}{\overline{I}_n} = \left[1 - \frac{L_p \frac{dI_n}{dt}}{V_{in} d(t_n) - mV_E} \right] \frac{mR_{LED} + R_{S_n}}{mR_{LED} + R_{S_n} + R_p} \tag{6.20}$$

In practice, equation (6.20) establishes the degree of depreciation of a LED string current, introduced by the parasitic components related to the long cabling. Knowing in advance that PWM dimming is commonplace, it is clear that the first term of (6.20) will be severely affected by the parasitic inductance L_p. This term, in turn, impacts on the sharpness of the waveform of the LED string current – square wave. On the other hand, the second term, which integrates the parasitic resistance R_p, suffers a relatively small influence from R_p, as $R_p << mR_{LED} + R_{S_n}$. Thus, the depreciation of the LED string current is mostly exacerbated by the parasitic inductance L_p. Also, equation (6.20) reveals that it is the manipulation of the dimming ratio that enables the most profitable compensation of current.

Determining the 'dimming ratio – maximum string current' pair that enables the most profitable current compensation reveals as a challenging task, particularly if performed manually. Alternatively, automatic determination of the two parameters reveals advantageous. The automatic current compensation strategy consists of the dynamic adaptation of the dimming ratio d_n and/or the maximum string current I_{max_n}. It may be developed through either the dynamic adaptation of a single parameter (the dimming ratio d_n or the maximum string current I_{max_n}) or through the concurrent adaptation of both parameters.

The dynamic dimming ratio, to be effectively imposed to each channel of the LED driver (d'_n) is computed taking into account the error between the expected average current and the effectively measured average current:

$$e = d_n I_{\max_n} - \overline{I}_n \tag{6.21}$$

$$d'_n = d_n + \int e \tag{6.22}$$

Identical rationale is followed for the computation of the maximum string current I'_{max_n}, which is the reference current to be effectively imposed to the sliding mode current controller:

$$I'_{\max_n} = I_{\max_n} + \int e \tag{6.23}$$

The error e is also obtained resorting to (6.21). The integration of the error aims to progressively reduces the error to zero.

6.2.2.2.1. Simulation results

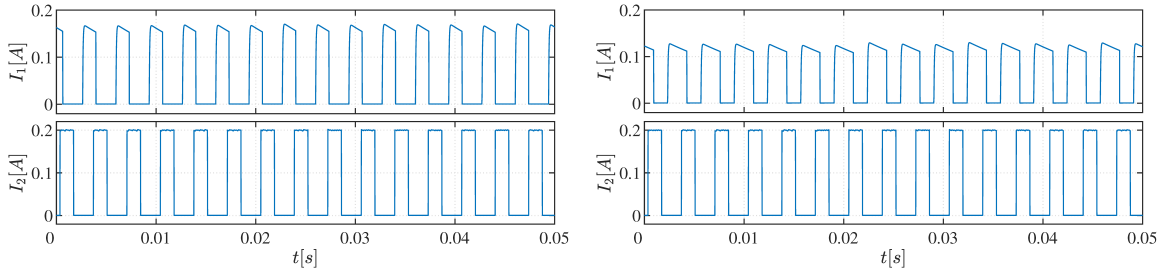
To validate the resiliency and effectiveness of the automatic compensation strategy, a simulation model was developed in *Simulink™* environment. The configuration of the model, along with the adopted parameters are described with detail in Appendix A.3. Three distinctive operation scenarios are defined. To observe the impact of the current compensation strategy in the presence of different cabling sizes, Scenario 1 considers the influence of a long cable only in String 1, represented in the simulation model by the parasitic components R_p and L_p. Please note that, for Scenario 1, the depreciation of the average current in the LED strings takes place not only because of the cable parasitics, but also because of an OC fault in switch S_1. As for Scenario 2, two distinctive dimming frequencies are adopted, in order to evaluate the impact of the parasitic components on the luminous flux of LEDs as a function of the dimming frequency. The reference currents and dimming ratios defined for each scenario are expressed in Table 6.7.

TABLE 6.7 PARAMETERS DEFINED FOR EACH OPERATION SCENARIO

	Scenario 1	***Scenario 2***	***Scenario 3***
Parameter	**Value**	**Value**	**Value**
S_1 fault?	Yes	No	No
Cable parasitics in String 1?	Yes	Yes	Yes
Cable parasitics in String 2?	No	Yes	Yes
$I_{max_n}[A]$	0.2	1	1
d_n	0.4	0.6	0.4
f_{dim} [Hz]	300	300, 1000	1000

For each operation scenario described in Table 6.7, the evaluation focused on the implementation of four distinctive conditions of compensation: 1) no compensation; 2) automatic compensation of d_n; 3) automatic compensation of I_{max_n}; 4) automatic compensation of both d_n and I_{max_n}. Data related to each of those four conditions is compiled in Table 6.8 to Table 6.11.

Fig. 6.22 depicts the currents flowing in String 1 and String 2, considering the operation conditions defined for Scenario 1 and automatic adaptation of the dimming ratio.



(a) (b)

Fig. 6.22 LED strings' currents, considering the conditions defined for Scenario 1: (a) without current compensation; (b) with current compensation through adaptation of the dimming ratio.

The joint effect of long cabling and an OC fault in switch S_1 seriously compromise the average current delivered to String 1, as demonstrated in Fig. 6.22 (a), dropping by 25 % of its original value. Such depreciation in the average current of String 1 is overcome, in great part, through the dynamic adaptation of the dimming ratio, as depicted in Fig. 6.22 (b). Indeed, the increment of the dimming ratio of current I_1 is noticeable in Fig. 6.22 (b). Table 6.8 provides detailed information about the implementation of each automatic compensation strategy. The column entitled "Ref. values" provides the values associated to each parameter under healthy converter operation, free from the influence of the cabling parasitics. Referring to Table 6.8, it is observed that the automatic adaptation of the dimming ratio successfully recovers great part of the expected average current of String 1. Indeed, dimming compensation provides the most significant contribution to the recovery of the original string current.

TABLE 6.8 SIMULATION RESULTS OBTAINED WITH AND WITHOUT DEPLOYMENT OF CURRENT COMPENSATION STRATEGIES, UNDER THE OPERATION CONDITIONS DEFINED FOR SCENARIO 1

Parameter	**Ref. values**	w/o comp.	w/ d'_n comp.	w/ I'_{max_n} comp.	w/ $d'_n + I'_{max_n}$ comp.
$\bar{I}_1$ [A]	0.080	0.060	0.071	0.062	0.073
d'_1	0.40	0.40	0.85	0.40	0.80
$\bar{I}_2$ [A]	0.080	0.080	0.080	0.077	0.080
d'_2	0.40	0.40	0.41	0.40	0.28

Table 6.9 and Table 6.10 provide numerical data related to Scenario 2. While Table 6.9 describes the operation of the LED lighting system at a dimming frequency of 300 *Hz*,

Table 6.10 compiles data related to the operation at a dimming frequency of 1000 *Hz*. The objective is to evaluate the impact of the variation of the dimming frequency on the attenuation of the LED strings' currents. After evaluating the results provided in Table 6.9 and Table 6.10, it is possible to take important remarks. Firstly, it is shown that the dimming frequency has significant impact on the attenuation of the LED strings' currents. Secondly, it is stated that dimming compensation, by itself, can effectively recover the original strings' current. Also, it is noted that the compensation based on automatic adaptation of the maximum string currents might not be effective in specific circumstances, and eventually lead to undesired over-currents, as shown in Table 6.9.

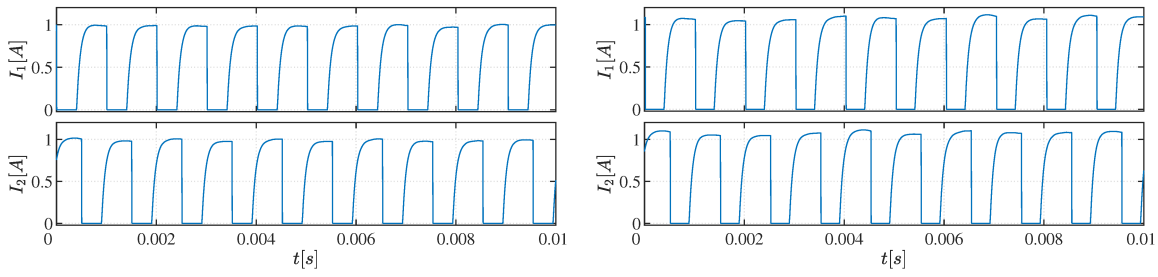
TABLE 6.9 SIMULATION RESULTS OBTAINED WITH AND WITHOUT DEPLOYMENT OF CURRENT COMPENSATION STRATEGIES, UNDER THE OPERATION CONDITIONS DEFINED FOR SCENARIO 2 (FDIM = 300 *HZ*)

Parameter	**Ref. values**	w/o comp.	w/ d'_n comp.	w/ I'_{max_n} comp.	w/ $d'_n + I'_{max_n}$ comp.
$\bar{I}_1$ [A]	0.600	0.567	0.600	0.625	0.600
d'_1	0.60	0.60	0.63	0.60	0.58
$\bar{I}_2$ [A]	0.600	0.568	0.600	0.624	0.600
d'_2	0.60	0.60	0.63	0.60	0.58

TABLE 6.10 SIMULATION RESULTS OBTAINED WITH AND WITHOUT DEPLOYMENT OF CURRENT COMPENSATION STRATEGIES, UNDER THE OPERATION CONDITIONS DEFINED FOR SCENARIO 2 (FDIM = 1000 *HZ*)

Parameter	**Ref. values**	w/o comp.	w/ d'_n comp.	w/ I'_{max_n} comp.	w/ $d'_n + I'_{max_n}$ comp.
$\bar{I}_1$ [A]	0.600	0.525	0.600	0.570	0.600
d'_1	0.60	0.60	0.67	0.60	0.63
$\bar{I}_2$ [A]	0.600	0.525	0.600	0.570	0.600
d'_2	0.60	0.60	0.67	0.60	0.63

Fig. 6.23 depicts the waveform of both LED strings' currents, considering the conditions defined for Scenario 2 and a dimming frequency of 1000 *Hz*.



(a) (b)

Fig. 6.23 LED strings' currents, considering the conditions defined for Scenario 2 and a dimming frequency f_{dim} = 1000 *Hz*: (a) without current compensation; (b) with current compensation through automatic adaptation of both dimming ratio and maximum string current.

Focusing on Fig. 6.23 (a), it is observed that the cable parasitics introduce a remarkable delay on the settling time of both LED strings' currents. The compensation of both dimming ratio and maximum string current introduce important improvements, as depicted in Fig. 6.23 (b). Numerical data related to the scenario depicted in Fig. 6.23 is provided in Table 6.10.

One of the direct consequences of the complex structure of the LED lighting system under evaluation is precisely the extensive set of parameters with impact on the performance of the system. For that reason, a third scenario of operation evaluates the system operation in the event that the dimming ratio falls below $100/n$ (i.e., 50 % for the LED lighting system under analysis). As shown in Table 6.11, the presence of the parasitic components cuts by half the average strings' currents. The proposed compensation strategies allow to effectively recover from such harsh depreciation of the current.

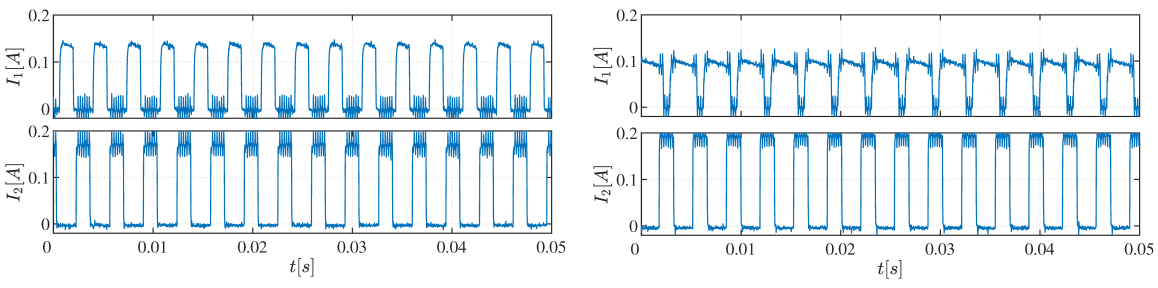
TABLE 6.11 SIMULATION RESULTS OBTAINED WITH AND WITHOUT DEPLOYMENT OF CURRENT COMPENSATION STRATEGIES, UNDER THE OPERATION CONDITIONS DEFINED FOR SCENARIO 3

Parameter	**Ref. values**	w/o comp.	w/ d'_n comp.	w/ I'_{max_n} comp.	w/ $d'_n + I'_{max_n}$ comp.
$\bar{I}_1$ [A]	0.400	0.202	0.400	0.203	0.400
d'_1	0.40	0.40	0.51	0.40	0.49
$\bar{I}_2$ [A]	0.400	0.202	0.400	0.203	0.400
d'_2	0.40	0.40	0.51	0.40	0.49

6.2.2.2.2. Experimental results

Experimental tests were conducted to confirm the effectiveness of the automatic current compensation strategy. The configuration of the system, along with the adopted parameters are described with detail in Appendix B.3. For the experimental validation, the operation conditions defined for Scenario 1 are considered. Given the limitations of the LED strings adopted in the experiments, with regards to their current ratings, the experimental tests did not embrace the conditions of Scenario 2 neither Scenario 3.

Fig. 6.24 depicts the currents flowing through each LED string, measured in the experimental tests.



(a) (b)

Fig. 6.24 LED strings' currents measured under the operation conditions defined for Scenario 1: (a) without current compensation; (b) with current compensation through dimming adaptation.

Overall, the experimental results shown in Fig. 6.24 are in agreement with the corresponding simulation results, shown in Fig. 6.22. As expected, some high-frequency noise is present in the waveforms of the LED strings' instantaneous currents I_1 and I_2. Such noise mainly finds its roots on the multiple switching mechanisms occurring in the LED driver. It is worth noting that the drop on the maximum value of I_1, observed in Fig. 6.24 (b), is a natural consequence of the automatic dimming adaptation. Such measure enables the compensation of both I_1 and I_2.

Table 6.12 compiles data related to the average current on the two LED strings, measured after the OC fault on switch S_1.

TABLE 6.12 EXPERIMENTAL RESULTS OBTAINED WITH AND WITHOUT DEPLOYMENT OF CURRENT COMPENSATION STRATEGIES, UNDER THE OPERATION CONDITIONS DEFINED FOR SCENARIO 1

Parameter	**Ref. values**	w/o comp.	w/ d'_n comp.
$\bar{I}_1$ [A]	0.080	0.053	0.076
d'_1	0.40	0.40	0.81
$\bar{I}_2$ [A]	0.080	0.070	0.080
d'_2	0.40	0.40	0.44

As confirmed in Table 6.12, the adoption of automatic dimming compensation successfully re-establishes the average current in all LED strings, without meaningful deviation from the expected average current. As expected, it is current $\bar{I}_1$ that drops the most because of the OC fault (33.75 %). The automatic dimming compensation amends both $\bar{I}_1$ and $\bar{I}_2$ to their original values.

6.2.2.3. Sensorless current control

As mentioned previously, SIMO LED drivers combine a plethora of key advantages over single-output LED drivers, namely the inherent tolerance against faults in the LEDs or in the current control switches, the optimised utilisation of resources, and the potential to decentralise the converter, placing it away from the LED strings.

Still, this LED driver configuration also suffers from important drawbacks. The assignment of individual current control loops to each one of the LED strings, as adopted in [36], [148], [149], enhances the complexity and cost of the entire lighting system, on the one hand, and creates an important barrier to the implementation of lighting systems with a decentralised driver, on the other hand. Moreover, the overall efficiency of the lighting system gets compromised, as a result of the insertion of current sensing resistors on each one of the LED strings. The adoption of a current control strategy based on the inclusion of multiple current sensing resistors negatively affects the overall efficiency and lifetime of the driver, since it incurs additional losses on the driver circuit. Indeed, the losses incurred by current sensing resistors may even represent the highest share among the overall losses of

a SIMO LED driver [149]. Hence, the elimination of the multiple current sensing devices from the SIMO converter should provide an effective mean to optimise the global efficiency of the lighting system. In addition to the optimisation of efficiency, the simplification of the current sensing mechanisms creates an excellent opportunity to ameliorate the reliability of the entire LED lighting system. Current sensing components show tremendous potential to fail, compromising the stability and quality of light.

To reduce the complexity of the current controller, alternative SIMO converter architectures adopt single-loop control configurations. In [150], the proposed current-source-mode SIMO converter assures that the converter outputs are independent, thus allowing to adopt a simpler single-loop current controller. Identical approach is adopted in [151], where multiple series-connected LED strings are supplied by a SIMO LED driver. These strategies are targeted at SIMO converter architectures containing a front-end current control stage, which greatly compromises the redundancy and, consequently, the reliability of the LED driver. On that basis, the state-of-art single-loop control approaches are ineffective for the fault-tolerant SIMO converter under consideration in this work.

The implementation of a sensorless current control strategy in multi-output LED drivers provides pivotal advantages in terms of optimisation of resources, efficiency improvement, and lifetime extension of the LED driver. Only the inductor current is monitored for current control purposes. The reference value of the average inductor current is generated resorting to the information about the dimming commands assigned to each converter channel [152].

Fig. 6.25 depicts the structure of the fault-tolerant SIMO LED driver, free of any current sensing elements.

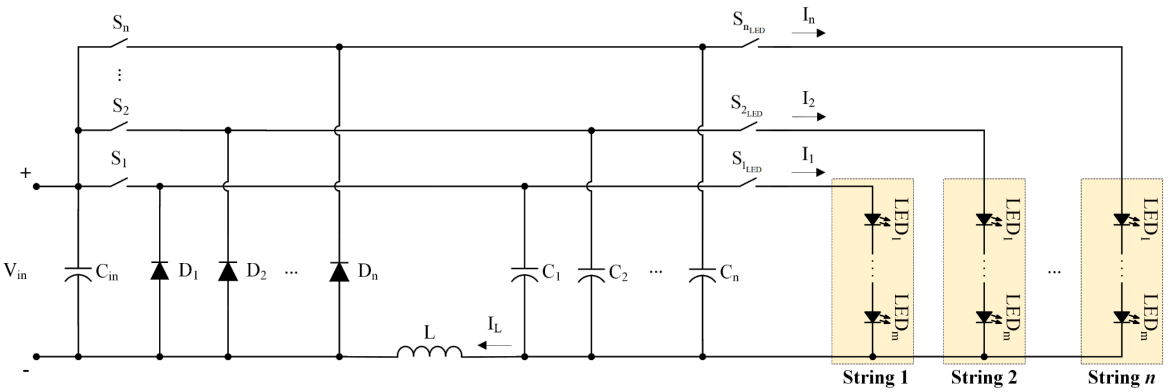


Fig. 6.25 Fault-tolerant SIMO LED driver, free of current sensing elements, adopted in the evaluation of the sensorless current control strategy.

The average current flowing through the converter inductor equals the average current at the converter output. As the SIMO LED driver comprises multiple outputs, the inductor average current, assessed for a certain period of time, is equal to the sum of the average currents measured, in that same period of time, in all the driver outputs:

$$\bar{I}_L = \sum_{1}^{n} \bar{I}_n = \sum_{1}^{n} \frac{1}{T} \int_{0}^{T} I_n \, dt \tag{6.24}$$

For the control strategy under evaluation, the intervals of interest are the ON-periods of the LED strings. In other words, the current controller must ensure that the LED strings' currents track the reference currents over those periods.

As the LED string currents remain constant, or at least suffer very small oscillations, during the ON-periods of the LED strings, it is fair to assume that the average LED strings' currents, assessed along the periods of interest, are equal to the instantaneous string currents:

$$\bar{I}_{1\ldots n} = I_{1\ldots n} \tag{6.25}$$

Based on (6.24) and (6.25), the average inductor current $\bar{I}_L$ results from the sum of the instantaneous string currents:

$$\bar{I}_L = \sum_{1}^{n} I_n \tag{6.26}$$

Thanks to the simplification made in (6.26), the control of the LED strings' currents gets greatly facilitated. Complex mathematical manipulations are obviated, as the average inductor current equals the sum of instantaneous currents.

As the adopted control variable is the average inductor current, the reference inductor current $I_{L_{ref}}$ is also a function of the reference currents of each LED string:

$$I_{L_{ref}} = \sum_{1}^{n} I_{n_{ref}} \tag{6.27}$$

To better understand the relation between the reference current $I_{L_{ref}}$ and the reference LED strings' currents, Fig. 6.26 shows a generic representation of the reference currents, defined for each LED string, in a three-output LED driver. The resulting reference inductor current $I_{L_{ref}}$ is the sum of the references associated to each LED string.

Average current control may rely on a multitude of strategies, with distinctive merits and complexity levels. In this study, the implementation of the average current control strategy relies on a precise control of the ON- and OFF-periods of the semiconductor assuring current control functions [153]. Two reference signals are introduced into the controller: the average and peak references of the inductor current.

The implemented current controller allows a hysteresis window of ± 10 % of the reference inductor current. Since the adopted hysteresis current control strategy relies on the control of both the average and peak currents, the reference for the inductor peak current

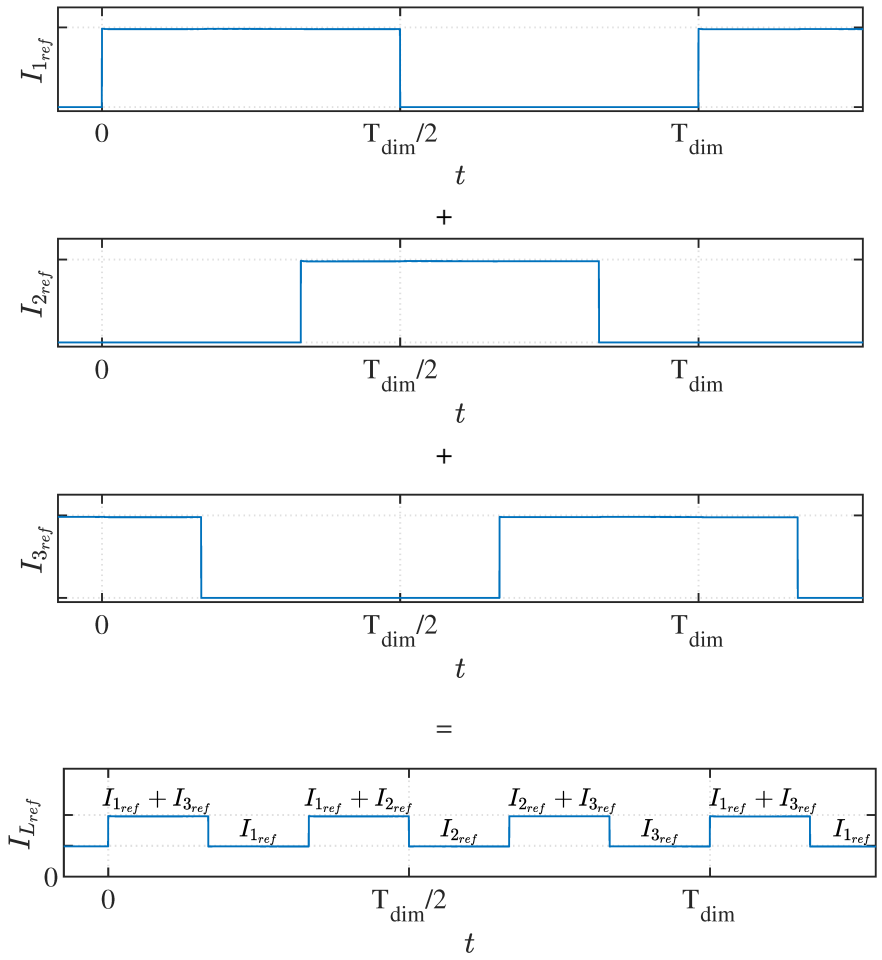


Fig. 6.26 Generic representation of the relation between the reference LED strings' currents $I_{1_{ref}} \dots I_{3_{ref}}$ and the resulting reference inductor current $I_{L_{ref}}$.

is obtained through the average inductor current reference $I_{L_{ref}}$:

$$I_{pk_{ref}} = 1.1 I_{L_{ref}} \tag{6.28}$$

Fig. 6.27 depicts a simplification of the sensorless current control strategy, suitable for application on a fault-tolerant SIMO LED driver composed of n channels. In the schematic, $S_{1_{LED}} \dots S_{n_{LED}}$ denote the dimming commands applied to the dimming switches of the fault-tolerant SIMO LED driver, whereas $S_{ts_1} \dots S_{ts_n}$ denote the time-sharing commands, which are internal variables of the controller. For further reference regarding time-sharing modulation signals and their characteristics, refer to Fig. 3.6.

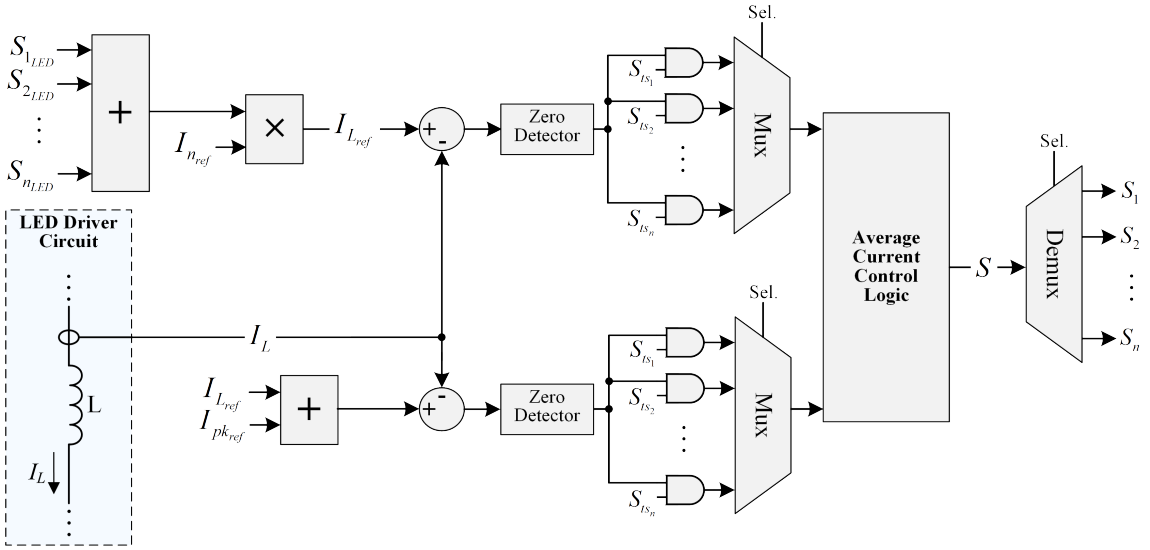


Fig. 6.27 Generic representation of the sensorless current control strategy, based on the average inductor current monitoring.

6.2.2.3.1. Simulation results

A simulation model, comprising the fault-tolerant SIMO LED driver depicted in Fig. 6.25 and the corresponding current controller, was developed in the software *Simulink™*, to verify the effectiveness of the sensorless current control strategy. Further information regarding the simulation model and the adopted parameters can be found in Appendix A.4.

The selected simulation scenarios consider the operation of the LED driver at distinctive current levels and dimming ratios, aiming to exploit the capability of the adopted LED driver to use the entire dimming range.

As requested in any LED lighting application, the controller should be able to ensure that the LED strings' currents successfully track the reference values, with minimal harmonic distortion. Observing these two important criteria is fundamental to ensure the ability of the LED lighting system to produce high-quality light, with minimal hazard for human health.

Fig. 6.28 depicts the waveforms of the three LED strings' currents, when a reference current of 0.5 *A* is imposed at the input of the controller. Each LED string adopts a distinctive dimming ratio. The dimming ratio d_{dim} is set at 0.2 for String 1, 0.5 for String 2, and 0.7 for String 3.

As confirmed in Fig. 6.28, the current is kept constant during the ON-period defined for each LED string, with null deviation from the reference value.

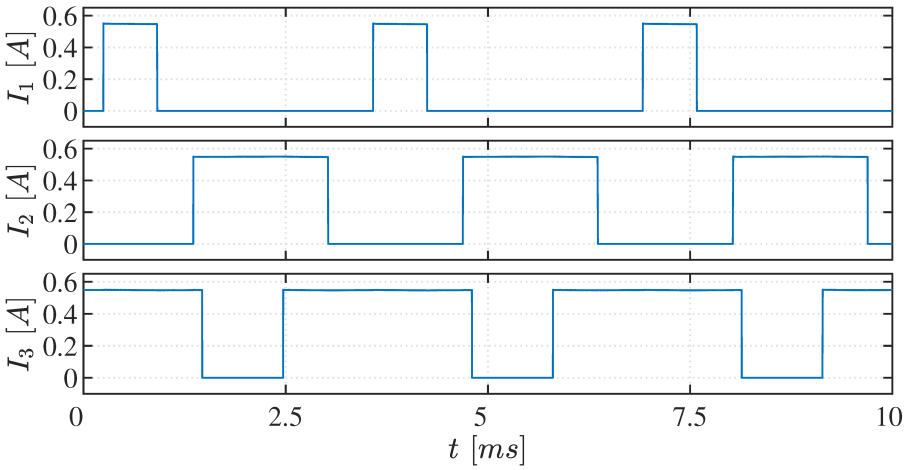


Fig. 6.28 Instantaneous currents measured in a three-string LED lighting system. The dimming ratio d_{dim} is 0.2 for string 1, 0.5 for string 2, and 0.7 for string 3. The current reference $I_{n_{ref}}$ is set at 0.5 A in all LED strings.

The response of the current controller is equally effective when higher load levels are imposed. Fig. 6.29 depicts the instantaneous LED strings' currents, measured on a three-output LED driver, when the string current is set at 2 A. All LED strings apply a dimming ratio d_{dim} of 0.2.

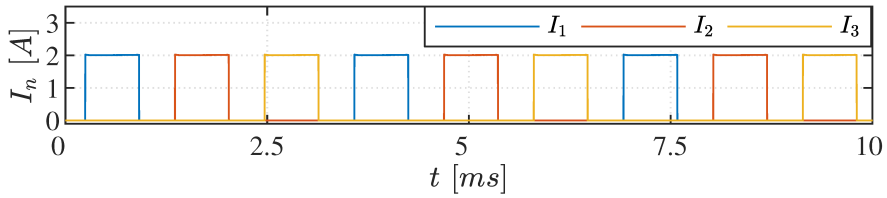


Fig. 6.29 Instantaneous currents measured in a three-string LED lighting system. The dimming ratio d_{dim} is 0.2 in all LED strings, while the current reference $I_{n_{ref}}$ is set at 2 A for all strings.

Just like in the first simulated scenario, Fig. 6.29 shows that the current flowing through each LED string is kept constant during the corresponding ON-period, with minimal shift from the imposed reference current. Indeed, Fig. 6.30 confirms that the proposed controller also has relevant merits in terms of dynamic response.

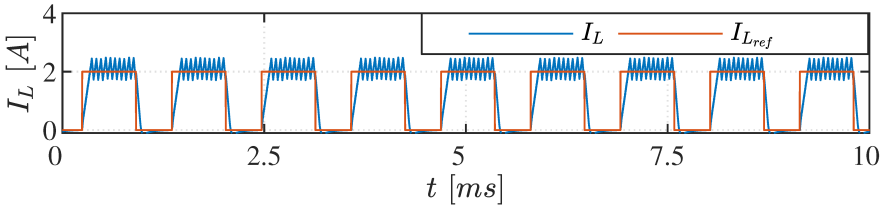


Fig. 6.30 Inductor current reference $I_{L_{ref}}$ versus instantaneous inductor current I_L, assessed for the operation conditions represented in Fig. 6.29.

The controller successfully tracks the imposed inductor current reference $I_{L_{ref}}$, exhibiting a short response time to step variations in the reference current. Note that the

sawtooth pattern observed in the inductor current, during the ON-periods, results from the converter switching action imposed by the hysteresis controller.

Precise current control is equally attained when all three LED strings adopt a significantly larger dimming ratio, as demonstrated in Fig. 6.31. For this scenario, a dimming ratio of 0.5 is imposed in all three LED strings.

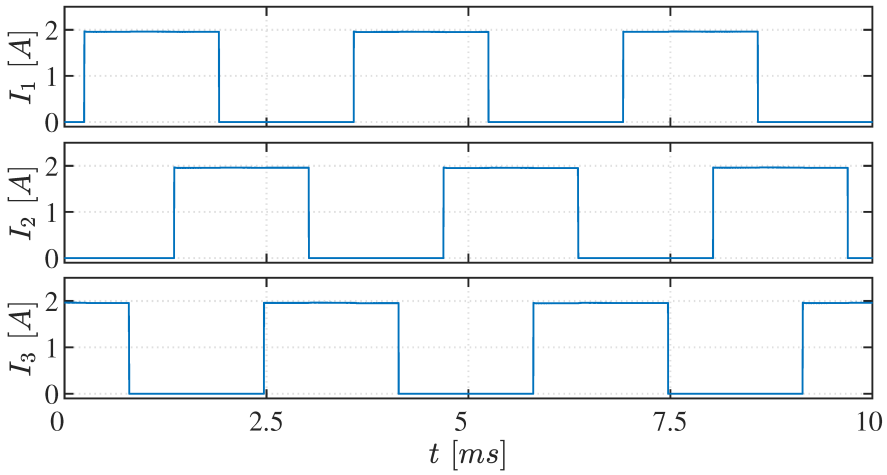


Fig. 6.31 Instantaneous currents measured in a three-string LED lighting system. The dimming ratio d_{dim} is 0.5 in all strings, while the current reference $I_{n_{ref}}$ is set at 2 A in all strings.

The three LED strings' currents successfully reach the imposed reference levels, even when heavy load conditions are imposed. The simultaneous activation of multiple LED strings does not introduce distortion into the waveforms of the LED strings' currents. Moreover, excellent levels of accuracy are attained for the operation conditions depicted in Fig. 6.31. A closer look over the current waveform of LED string 1 (I_1) is provided in Fig. 6.32.

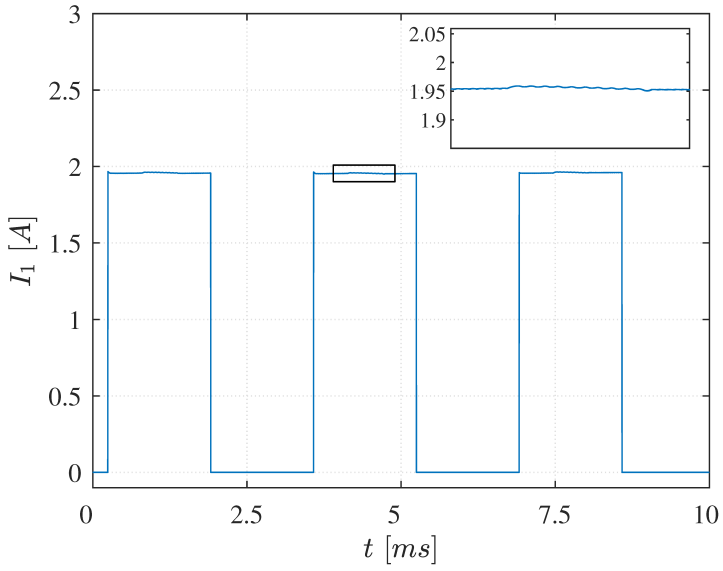


Fig. 6.32 LED string 1 current, including a zoomed view of the waveform, assessed for the operation scenario presented in Fig. 6.31.

The excellent performance indicators related to the sensorless current control strategy are extended to the operation of the LED driver under dynamic load conditions, as confirmed in Fig. 6.33. With the proposed current controller, the string currents $I_{1...3}$ successfully reach the updated reference current in less than 20 *ms*.

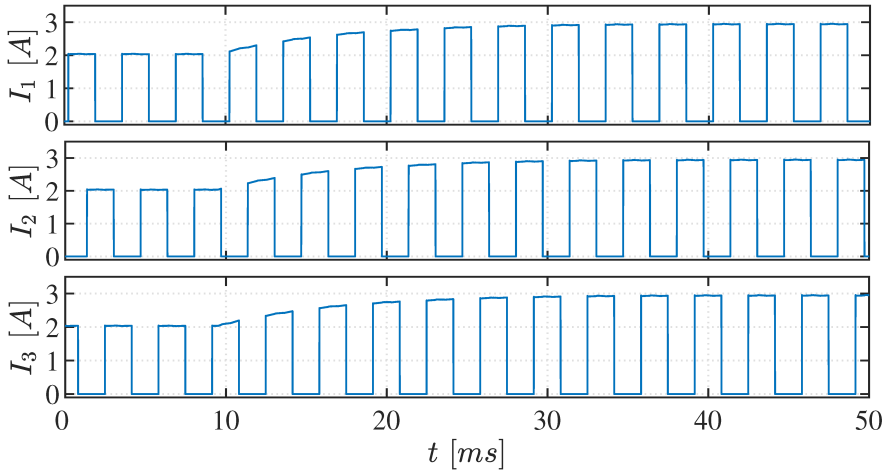


Fig. 6.33 Instantaneous LED strings' currents measured for a three-string LED array. The current reference $I_{n_{ref}}$, initially set at 2 *A*, is increased to 3 *A* in all strings, at t = 10 *ms*.

One of the most important virtues that any current controller targeted at LED lighting applications should comply with is the ability to develop highly accurate current control. To evaluate the degree of effectiveness of the sensorless current control strategy, it becomes critical to obtain a metric of accuracy. The accuracy of the current controller is assessed through the LED strings' current error ΔI_n, which results from the difference between the reference current $I_{n_{ref}}$ and the effective LED strings' current I_n:

$$\Delta I_n[\%] = \frac{I_{n_{ref}} - I_n}{I_{n_{ref}}} \times 100. \tag{6.29}$$

Results reported in the literature show that LED drivers implementing the most recent current control strategies provide accuracy levels ranging from 2 % to 5 % [154].

Resorting to the simulation results obtained for the sensorless current controller, Fig. 6.34 establishes the relation between the dimming ratio and the resulting error ΔI_n, considering three distinctive levels for the LED strings' current reference.

As confirmed in Fig. 6.34, the sensorless current controller provides accurate current control, showing performance levels comparable to those of state-of-the-art current controllers with multiple control loops and current sensing elements. Important improvements in the controller accuracy are attained as the dimming ratio increases, particularly for the scenarios when $I_{n_{ref}}$ is equal to 0.5 *A* and 1 *A*. It is equally interesting to observe that the sensorless controller provides highly accurate current control when the

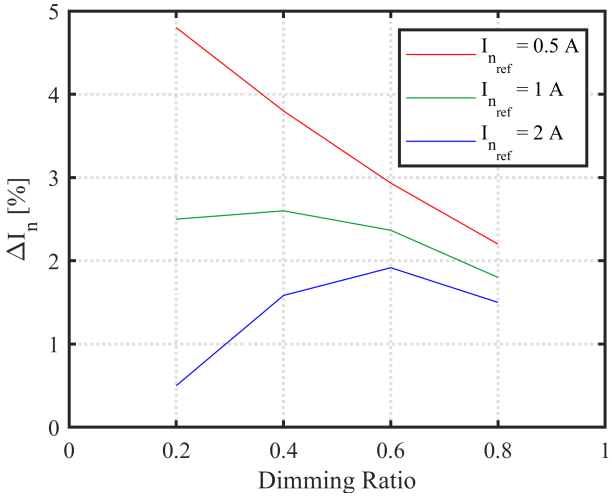


Fig. 6.34 LED strings' current error ΔI_n as a function of the dimming ratio, considering three distinctive LED strings' current references.

current reference is set at 2 A. For such condition, the error ΔI_n is kept below 2 % for the entire dimming range of the LED driver, thus confirming the ability of the sensorless current control strategy to outperform the state-of-the-art solutions in the entire range of operation, with regard to accuracy.

Chapter 7

Power conversion technologies for DC-supplied homes and offices: performance analysis and comparison

The adoption of DC microgrids within the context of homes and offices provides key answers to some of the most critical challenges faced by mankind nowadays, namely the compelling need for more efficient and reliable use of energy. But the transition towards a scenario of wide adoption of DC microgrids also poses a significant set of technical hurdles that remain unsolved. One of those hurdles is precisely the selection of the proper technologies/solutions for each one of the building blocks of the microgrid.

DC–DC power converters are perhaps the most important elements of any DC microgrid. The scientific literature reports a multitude of DC–DC converter topologies, with particular merits. Still, most of them have not been evaluated nor optimised in the context of DC microgrids. For that reason, a careful and weighted analysis of the performance of candidate converter topologies to fulfil the requirements of each practical application is of paramount relevance.

To take enlightened decisions about the most suitable converter topologies for each end-use, following sections provide a comparative evaluation of the performance of candidate converter topologies, revealing most suitable features for the most relevant end-uses found in residential buildings and offices. This thesis devotes particular attention to the most representative end-uses: EV charging, LED lighting, and general appliances. Along each section, data from the state-of-the-art is presented, followed by an evaluation of parameters deemed suitable to assess the performance of two potential candidate DC–DC converters per application. The performance of each converter topology is evaluated resorting to parameters such as efficiency, cost of ownership, or tolerance against faults.

7.1. EV charging

A multitude of DC–DC converter topologies, employed in EV charging applications, have been reported in the literature [155], [156]. Given the prevalence of AC-based energy

distribution systems, most of these DC–DC converters are integrated into multi-stage power conditioning systems, where they develop power factor correction, charging regulation, and/or galvanic isolation functions [157].

Review studies devoted to EV charging technologies provide an extensive look over the multitude of architectures proposed in the literature for EV charging applications. In [157], the discussion addresses a broad range of architectures, including the chargers based on classical PFC AC–DC rectifiers, isolated DC–DC converters, and the integrated single-stage converters. The review study developed in [158] presents the power conversion solutions typically considered for DC fast charging stations. Systems supplied through single-phase and three-phase AC power supplies are presented. Also, chargers integrating both non-isolated and isolated DC–DC converters are considered there. Charging solutions based on multilevel converters, considered some of the newest power conversion technologies, are the focus of the review provided in [159].

Non-isolated DC–DC converters offer simple and low-cost power conversion solutions for EV charging applications, capable of attaining high conversion efficiency, providing important advantages over isolated DC–DC converters [160]. When it concerns to non-isolated DC–DC converter topologies, the preference typically falls upon two specific topologies. While some literature selects interleaved DC–DC converters as the preferable topology for EV charging applications [161]–[164], other studies adopt multilevel DC–DC converters as the topology of choice [159], [165], [166].

Within the multitude of DC–DC converters described in the literature, the bidirectional configurations of the interleaved converter and multilevel converter appear as the most prominent solutions envisioned for DC-supplied EV charging systems to install at homes and offices. Accordingly, following sub-sections provide a parametric comparison between the two topologies, aiming to establish the preferrable solution [167].

7.1.1. Converter topologies

Fig. 7.1 depicts the structure of the two DC–DC converter topologies adopted for the comparative analysis. The first converter consists of a three-phase interleaved bidirectional DC–DC converter, while the second converter consists of a three-level multilevel bidirectional DC–DC converter.

The selection of these two converter topologies aims to answer to the requirements of EV charging systems for homes and offices in terms of efficiency, cost, and ability to handle high power ratings. These two DC–DC converter topologies provide key benefits like the fairly simple hardware architecture, the ability to effectively control the power flows in two directions (G2V and V2G), and the scalable architecture. It is worth mentioning that the

selection of the converters phases/levels relies on a compromise between complexity of the converters hardware and the system power ratings.

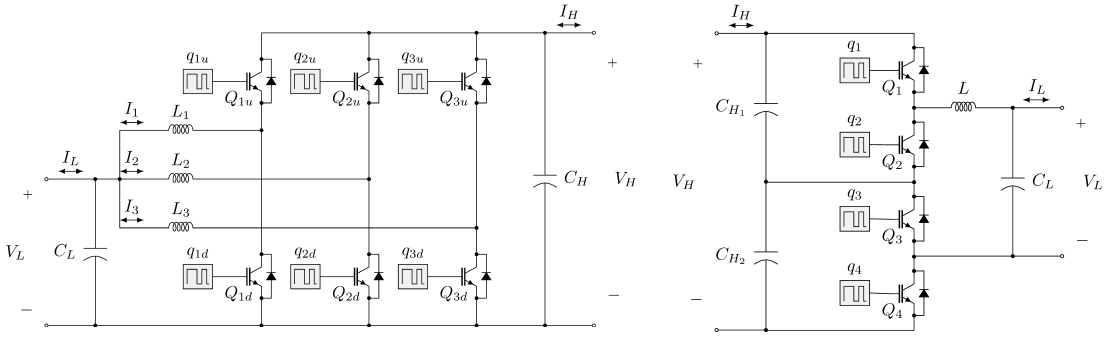


Fig. 7.1 DC–DC converter topologies adopted for the comparative analysis: (a) interleaved bidirectional DC–DC converter; (b) multilevel bidirectional DC–DC converter.

To assist in the evaluation of each topology, simulations are developed resorting to software *Simulink™*. The performance of each converter topology is tested considering the charging procedure of ESSs with the same specifications for both converter topologies. Table 7.1 specifies the parameters of the power semiconductors and other discrete components employed in the converters, as well as the characteristics of the power supply and EV ESS, based on a Li-ion battery pack. The characteristics of the power semiconductors are those of the Semikron SKiiP 132 GD 120 - 318 CTV power module.

TABLE 7.1 SYSTEM PARAMETERS

Parameter	Value
Input voltage	380 *V*
IGBT ON resistance	14.7 *mΩ*
IGBT forward voltage	1.38 *V*
Free-wheeling diode ON resistance	5.7 *mΩ*
Free-wheeling diode forward voltage	0.91 *V*
Battery pack rated voltage	140 *V*
Battery pack capacity	223 *Ah*

7.1.2. Performance comparison

7.1.2.1. Fault tolerance

The fault tolerance of the selected converter topologies is defined according to the ability of the converter to sustain the continuous supply of energy to the EV energy storage system (ESS), even in case of failure of sensitive components of the EV charger, without resorting to redundant elements. Fault tolerance gains particular relevance in EV charging applications, given the compelling need to assure continuous operation of the EV charging while keeping all components involved in the operation free of potentially hazardous perturbations.

For the interleaved DC–DC converter, an OC fault in any of the active switches does not impact the capability of the power converter to sustain the charging procedure. If the converter control remains unchanged during the post-fault period, the same amount of power is still transferred to the ESS, at the expense of additional harmonic distortion on the converter input and output currents. As it has been addressed previously on this thesis, there are a multitude of reconfiguration strategies available in the literature that can effectively overcome such challenge.

On the other hand, it is observed that most multilevel converter architectures are unable to provide fault-tolerant operation. In the case of the three-level bidirectional converter, fault-tolerant operation cannot be achieved at all, neither in buck nor boost operation mode. Only a few specific failure modes of higher-order multilevel converters – as it is the case of the five-level converter – allow to sustain the operation in degraded mode and, consequently, provide continuous charging of the ESS.

7.1.2.2. Components stress

The peak voltage and peak current imposed to the individual converter components are commonly adopted metrics to assess the stress imposed to the converter components [168].

While developing a stress analysis, particular attention should be devoted to the stress imposed to the most sensitive components. In power electronics systems, power semiconductors and capacitors are among the most sensitive components, showing the highest failure rates [169]. Compliance with the current ratings of the active switches is perhaps the most critical aspect to take into account.

Table 7.2 lists the parameters used to assess the stress imposed to the components of each DC–DC converter topology.

TABLE 7.2 STRESS IMPOSED TO THE CONVERTER COMPONENTS

Parameter	Interleaved Converter	Multilevel Converter
Switches voltage (V_Q)	V_H	V_H / (n - 1)
Diodes voltage (V_D)	V_H	V_H / (n - 1)
Inductor(s) voltage (V_L)	V_L	V_L
High-voltage side capacitor(s) voltage (V_{C_H})	V_H	V_H / (n - 1)
Low-voltage side capacitor voltage (V_{C_L})	V_L	V_L
Switches current (I_Q)	I_L / n	I_L
Diodes current (I_D)	I_L / n	I_L
Inductor(s) current (I_L)	I_L / n	I_L

*__Nomenclature:__ n – number of converter phases/levels

Data provided at Table 7.2 shows that the multilevel converter has inherent advantages when compared to the interleaved converter with regard to voltage stress imposed to the most sensitive components - power semiconductors and capacitors. For the three-level converter, the voltage stress imposed to those components is half of the high DC bus voltage V_H. Meanwhile, the peak voltage imposed to the power semiconductors and diodes of the interleaved converter is equal to V_H, regardless of the number of converter phases.

On the other hand, the interleaved converter provides important advantages in comparison to the multilevel converter when it concerns to current stress imposed to the switches and diodes. The current stress imposed to those components is inversely proportional to number of phases of the interleaved converter.

7.1.2.3. Components count

The number of components required to build a DC–DC converter is another relevant performance metric, as it has direct influence on the volume and cost of the system. The number of components is defined through a generic count, based on the number of converter phases (for the interleaved converter) and on the number of converter levels (for the multilevel converter). Both active and passive components account for the total number of components of the converter. Table 7.3 establishes a comparison between the two topologies, in terms of components required to build a n phase / n level converter.

TABLE 7.3 NUMBER OF CONVERTER COMPONENTS

Parameter	Interleaved Converter	Multilevel Converter
Switches	$2n$	$2n$ - 2
Diodes	$2n$	$2n$ - 2
Inductors	n	1
Capacitors	2	n
Total no. of components	$5n$ + 2	$5n$ - 3

*__Nomenclature:__ n – number of converter phases/levels

Overall, the multilevel converter obviates the requirement of 5 components, in case that a comparison between a n multilevel converter and a n interleaved converter is established. Looking at the components level, it is observed that the multilevel converter requires fewer semiconductors than the interleaved converter. Only one inductor is employed in the multilevel converter, while the interleaved converter employs one inductor for each phase. On the other hand, it is the interleaved converter that employs fewer capacitors (only 2); the multilevel converter requires n capacitors.

7.1.2.4. Cost effectiveness

One of the most straightforward and effective means to evaluate the cost effectiveness of power conversion systems consists of establishing an estimation of the cost of ownership associated to each converter topology. To that end, a simplified estimation of the cost of ownership is established, including the costs of the active and passive components of each converter topology.

The selection of the converter components takes into account the requirements of a 7 *kW* low-voltage power converter, based on each one of the topologies under study. The following components have been considered for the cost analysis:

Three-Phase Interleaved Converter:

- *Switches + Diodes:* ON SEMICONDUCTOR, IGBT Single Transistor, General Purpose, 40 A, 600 V, 165 W, 600 V, TO-247AB, 3 Pins;
- *Inductors:* Hammond Manufacturing Fixed Inductor, 1 mH, 20 A, Model 195C20;
- *Capacitors:* Electrolytic Capacitor, Snap-in, 680 µF, 400 V, B43547 Series, 8000 hours @ 105°C, ± 20%.

Three-Level Multilevel Converter:

- *Switches + Diodes:* ON SEMICONDUCTOR, IGBT Single Transistor, General Purpose, 120 A, 600 V, 600 W, 600 V, TO-247AB, 3 Pins;
- *Inductors:* Hammond Manufacturing Fixed Inductor, 2.5 mH, 50 A, Model 195E50;
- *Capacitors:* Electrolytic Capacitor, Snap-in, 680 µF, 200 V, 157 PUM-SI Series, 5000 hours @ 85°C, ± 20%.

Table 7.4 provides a simplified estimation of the cost of ownership associated to each converter topology, developed with the abovementioned components. The presented estimation is based on a query to potential suppliers of electronic components, carried out on the 29th of February 2020.

TABLE 7.4 COST OF OWNERSHIP

Parameter	Interleaved Converter	Multilevel Converter
Switches + Diodes	22.08 €	20.96 €
Inductors	155.22 €	238.27 €
Capacitors	14.60 €	16.12 €
Total cost	191.90 €	275.35 €

According to the data provided in Table 7.4, the selection of the interleaved converter provides relevant advantage in terms of cost of ownership. For the conditions considered in this thesis, the interleaved converter costs 30.3 % less than the multilevel converter. Such difference in the cost lies on the passive components, but particularly on the inductors

required for each topology. The single, high-current inductor employed in the multilevel converter represents an additional cost of around 83.5 €, in comparison to the total cost of the inductors required to build the interleaved converter. In opposition, the smaller, low-current rating inductors applied to each phase of the interleaved converter constitute a cheaper option.

The difference observed between the two architectures, in terms of cost, emphasise the importance of a careful design of the power converters and selection of the passive components of DC–DC converters.

7.1.2.5. Conversion efficiency

To assist on the determination of the efficiency of each topology, the two converters were tested over a broad range of operation conditions, taking profit of the developed simulation models. Fig. 7.2 shows the efficiency maps obtained for the two DC–DC converter topologies adopted for the comparative analysis. For each map, the efficiency is provided for multiple 'switching frequency-charging power' pairs. The range of switching frequencies and charging power considered in the efficiency maps takes into account the typical operation conditions of low- to medium-power charging systems adopted at residential buildings.

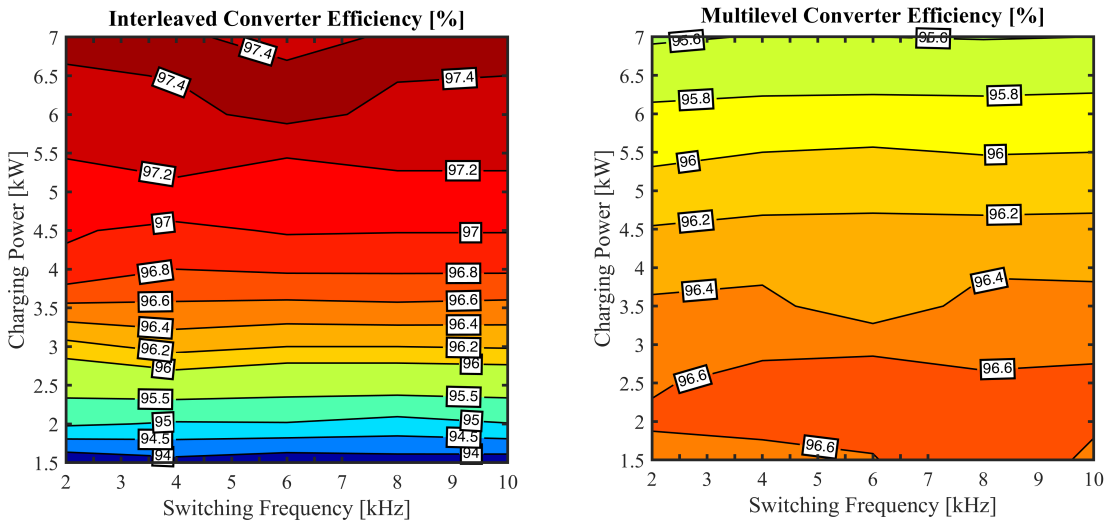


Fig. 7.2 Efficiency maps obtained as a function of the switching frequency and charging power, for the selected converter topologies: (a) interleaved bidirectional DC–DC converter; (b) multilevel bidirectional DC–DC converter.

The results shown in Fig. 7.2 provide useful information on the performance of the two converter topologies. Firstly, it is confirmed that the variation of the switching frequency does not have, in general terms, a relevant impact on the efficiency of both converter topologies. Also, it is stated that the interleaved converter shows superior efficiency levels in comparison to the multilevel converter, when the charging power sets

above 3.5 *kW*. Therefore, the interleaved converter provides superior performance when high-power charging is adopted.

On the other hand, it is interesting to notice that the multilevel converter provides the preferable choice when a variable charging power profile is requested. In other words, the multilevel converter provides a very uniform efficiency distribution along the entire range of charging power (1.5 *kW* to 7 *kW*).

To understand how the efficiency of each converter topology depends on the number of phases/levels, Fig. 7.3 shows the efficiency maps obtained for each converter topology, as a function of the number of phases/levels.

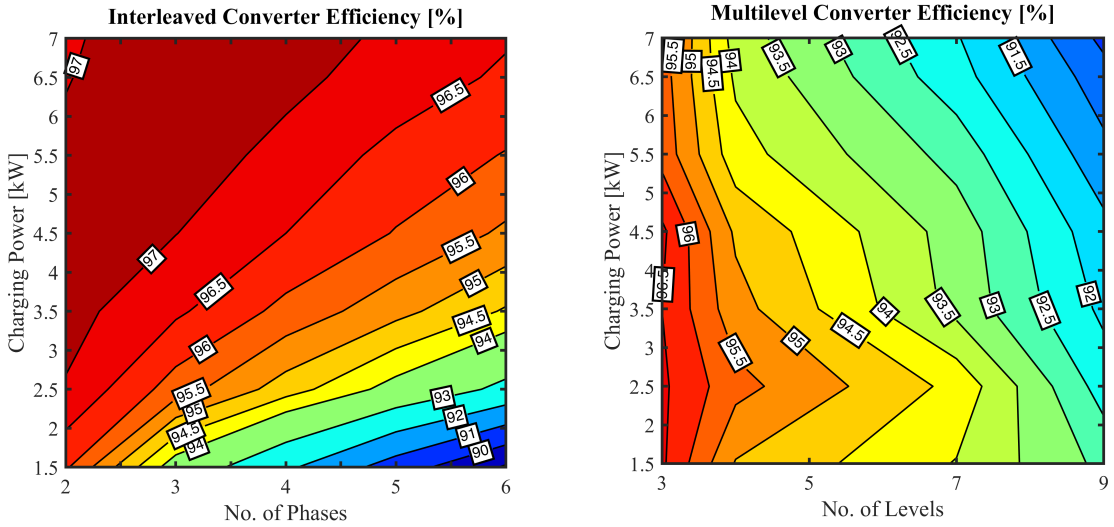


Fig. 7.3 Efficiency maps obtained as a function of the number of converter phases/levels, for the selected converter topologies: (a) interleaved bidirectional DC–DC converter; (b) multilevel bidirectional DC–DC converter. The switching frequency is kept constant, and set at 5 *kHz*.

The results of Fig. 7.3 show that lower-order derivations of the interleaved and multilevel converters have improved performance. Such behaviour takes place due to the reduced number of components required to build those derivations of the converters, allowing to reduce the overall conduction and switching losses.

Focusing the analysis on the interleaved converter, it is observed that the efficiency of the converter suffers a progressive degradation when the number of converter phases sets above 4. With regards to the multilevel converter, it is noticed that there is a direct correlation between the number of converter levels and the efficiency. The selection of 7-level and higher-order converter configurations appears to be disadvantageous, in terms of efficiency.

7.1.3. Analysis of results

Based on the analysis of multiple parameters, it is concluded that both topologies provide interesting merits. The full exploitation of such merits should carefully consider the

conditions in which the charging procedure takes place. In case that preference is given to cost effectiveness, conversion efficiency at high power levels, low current stress, and fault tolerance, the interleaved converter should be seriously considered as the topology of preference for the development of EV chargers based on DC–DC converters.

On the other hand, the multilevel converter shall be considered in case that preference is given to the implementation of EV chargers designed to operate at variable charging power, while imposing the voltage stress imposed to the converter components.

In conclusion, a global evaluation and weighting of the performance criteria allows to state that the interleaved bidirectional DC–DC converter has potential to become as the most appealing and interesting solution for DC-supplied residential EV charging systems.

7.2. LED lighting

The scientific literature also reports a multitude of DC–DC power conversion solutions suitable to drive LED lighting systems. Such solutions are generally integrated within AC–DC power conversion systems consisting of multiple power converters displaced in a cascaded configuration. Derivations of the SIMO converter [28], [36], non-resonant non-isolated buck converter [170], [171], flyback converter [33], [172], and resonant converter [173], [174] are some of the examples of a broader range of power conversion solutions that were reported in the literature lately as candidates for adoption in residential LED lighting systems. Most of the listed configurations are designed to supply multiple LED strings, through the integration of multiple channels, resorting to a single power converter. Some of the converters listed above have been evaluated through individual performance studies, without establishing comparisons among them.

The preference for LED drivers with multiple outputs typically arises in the context of large-scale lighting systems or high-power lighting systems. Under such circumstances, the adoption of centralised LED driver configurations provides important advantages over distributed LED driving configurations, with regards to maintenance, replacement of components, and efficiency. DC–DC converters based on the SIMO architecture are commonly selected when a centralised power converter is required to simultaneously supply multiple strings [36], [37].

Usually, the LED driver architectures described in the literature are not specifically designed for DC-based energy systems. Besides considering a complex power conversion architecture, made of AC–DC and DC–DC converters organised in cascade, the performance of LED drivers is not well understood nor optimised when they are supplied through DC microgrids.

Among the broad range of solutions available in the literature, the most prominent converter topologies envisioned for LED lighting systems to install at homes and offices,

supplied through DC microgrids, are the SIMO and the buck converters. Accordingly, following sub-sections describe a comparative study between the two topologies, aiming to establish the preferrable solution for residential LED lighting systems supplied through DC microgrids [175].

7.2.1. Converter topologies

This study focuses attentions on two simple LED driver configurations, suitable for residential lighting applications, capable of concurrently supplying multiple LED strings: the multiple-output buck converter, depicted in Fig. 7.4, and the SIMO converter, depicted in Fig. 7.5. Each LED driver is composed of *n* channels supplying *n* identical LED strings. In turn, each string is composed of an arrangement of *m* LED devices connected in series. For simulation purposes, the LED devices are modelled according to their approximated equivalent model [146]. For clarification, it is relevant to refer that the number of channels

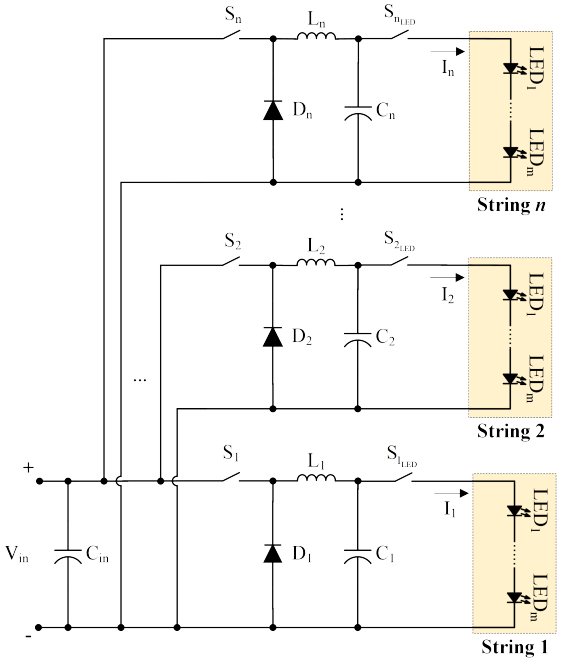


Fig. 7.4 Multiple-output LED driver based on multiple buck converters.

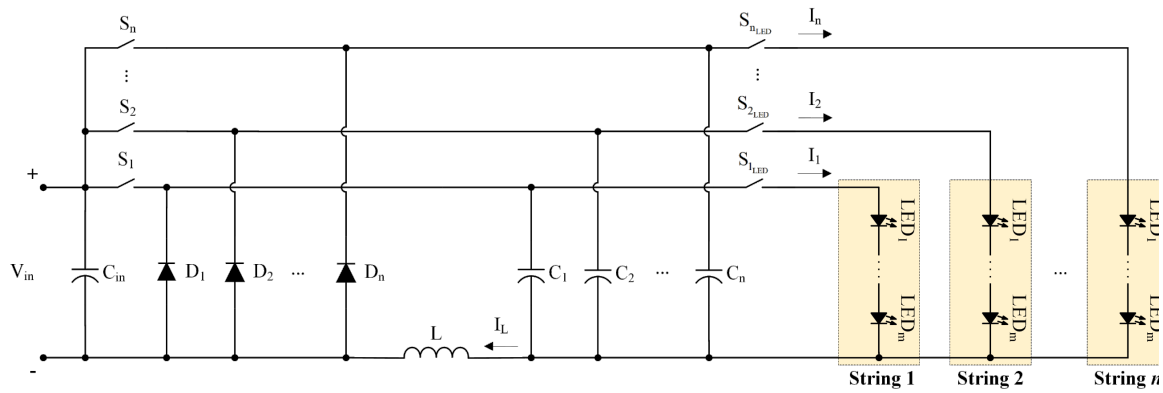


Fig. 7.5 Multiple-output LED driver based on the fault-tolerant SIMO converter.

of any LED driver is equal to the number of outputs, i.e., the number of LED strings it supplies.

Table 7.5 compiles the parameters of the drivers' components, while Table 7.6 includes information about the operational conditions considered for both LED drivers.

TABLE 7.5 SYSTEM PARAMETERS

Parameter	Nomenclature	Value
MOSFET ON resistance	$R_{DS_{on}}$	16 $m\Omega$
Inductance	$L_{1...n}$	7.6 mH
Inductor parasitic resistance	$R_{L_{1...n}}$	0.15 Ω
Free-wheeling diode ON resistance	$R_{D_{1...n}}$	10 $m\Omega$
Free-wheeling diode forward voltage	$V_{D_{1...n}}$	0.8 V
Output capacitance	$C_{1...n}$	200 μF
Output capacitor parasitic resistance	$Rc_{1...n}$	100 $m\Omega$
Sensing resistor	$Rs_{1...n}$	2 Ω

TABLE 7.6 OPERATION PARAMETERS

Parameter	Nomenclature	Value
Input voltage	V_{in}	380 V
LED string nominal voltage	$V_{n_{nom}}$	48 V
LED string nominal current	$I_{n_{nom}}$	0.22 A
LED string nominal power	P_{nnom}	11 W
Switching freq. (time multiplexing function)	f_t	5 kHz
Switching freq. (dimming function)	f_{dim}	300 Hz

Following sub-sections provide a comparative performance evaluation of the two topologies, considering parameters like fault tolerance, conversion efficiency, and cost of implementation. To assist on the evaluation of each topology, converters of the two topologies have been designed and modelled in simulation environment. For a fair comparison between the two configurations with regards to converter architecture as well as control performance, both LED drivers employ a time-sharing modulation strategy, being the current control developed by an hysteresis approach, as described in [143].

7.2.2. Performance comparison

7.2.2.1. Fault tolerance

The fault tolerance of the selected converter topologies depends on their ability to sustain the continuous supply of energy to the LED devices, without introducing significant distortion on the current, even in case of failure of particular components of the LED driver.

The literature reports that semiconductors and capacitors are the prevailing sources of failures in power electronic converters [169], as it is the case of LED drivers. For semiconductors, OC and SC faults are the prevailing failure modes. In fact, SCs faults generally lead, at a later stage, to OC faults.

To compare the response of the LED drivers in the presence of an OC fault of switch S_1, Fig. 7.6 depicts the waveforms of the current in LED string 1, assessed for two-channel configurations of each LED driver architecture considered in the study. The OC failure takes place at $t = 0.02\ s$. The waveforms of the current in LED string 2 are not included since their evolution is not affected by the failure.

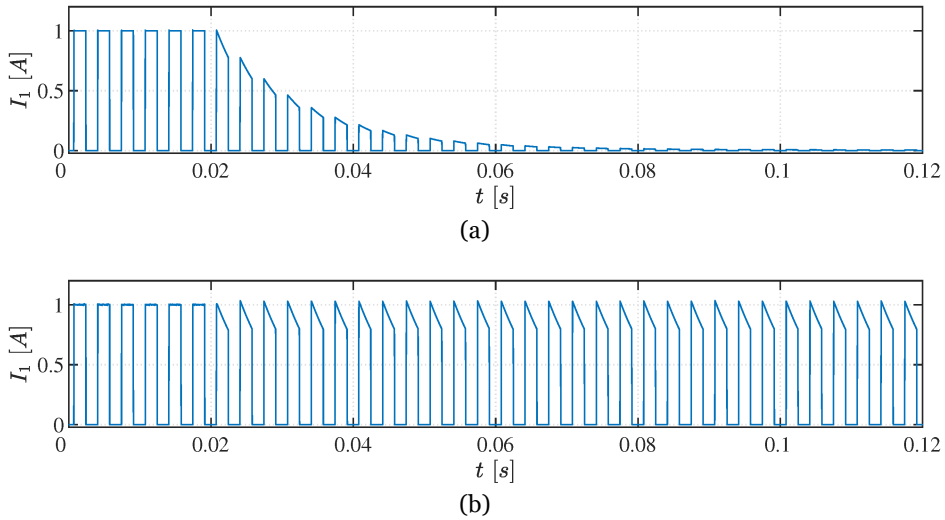


Fig. 7.6 Evolution of the current in LED string 1 in case of OC fault of switch S_1, observed for the two LED driver configurations: (a) multiple buck converters; (b) SIMO converter. An OC failure takes place at $t = 0.02\ s$.

With regards to the LED driver based on multiple buck converters, it is known that such configuration has inherent redundancy, given its modularity. As each LED string is controlled with a dedicated buck converter, the operation of each LED string solely depends on the health condition of the buck converter supplying it. In practice, such statement means that a failure in a single power semiconductor precludes the operation of the corresponding LED string, with complete loss of luminous flux in that LED string. The remaining strings remain fully operational, without loss of luminous flux nor perturbations in the quality of light, such as flicker. In case of an OC failure in the power semiconductor S_1 of the LED driver depicted in Fig. 7.4, LED string 1 will no longer produce light, while the remaining LED strings will remain fully functional – refer to Fig. 7.6 (a). Identical behavior will also take place in case of an OC failure of the power semiconductor $S_{1_{LED}}$.

One of the most relevant features of the SIMO LED driver, depicted in Fig. 7.5, is precisely the use of a single inductor, inserted in such a position of the power converter that enables its exploitation by all the converter channels, even in case of failure of any power

semiconductor. In practice, a failure of any power semiconductor developing current control functions (S_1 … S_n) does not compromise the operation of any LED strings. All LED strings continue to receive current and, thus, to produce light. Only the LED string connected to the faulty driver channel suffers a minor depreciation of the luminous flux – refer to Fig. 7.6 (b). Also, it is likely to observe higher harmonic distortion on the current delivered to the LED string associated to the faulty driver channel, because of the fault.

As confirmed in Fig. 7.6, the OC fault has distinctive effects on the response of the LED lighting systems. While the OC on switch S_1 of the buck converter represents a total depreciation on the current delivered to LED string 1 – Fig. 7.6 (a) – the same failure mode on the SIMO converter has limited impact on the current delivered to LED string 1 – Fig. 7.6 (b). Therefore, the SIMO converter provides an important advantage over the buck converter, ensuring improved availability of the entire lighting system.

Focusing on the SIMO LED driver and its operation over the post-fault period, it is clear that the OC fault introduces a depreciation on the average string current and, consequently, a depreciation on the luminous flux. In the case considered in Fig. 7.6, the average current drops from 0.5103 *A* to 0.4628 *A*, representing a depreciation of 9.3 % on the average string current. In practice, these numbers reveal the excellent ability of the SIMO LED driver to sustain the supply of energy to all outputs, even without deploying any reconfiguration strategies.

SIMO LED drivers usually rely on time-sharing modulation strategies to evenly share the inductor among all the driver channels. In the very few references found in the literature dealing with the reconfiguration of fault-tolerant LED drivers [146], the proposed strategies do not exploit the operation of the healthy switches with current control functions over the entire time range, by reassigning the timeslots left free by the faulty switch to the healthy ones. By doing so in the SIMO converter under evaluation, it is possible to fully banish the consequences of the fault, as shown in Fig. 7.7.

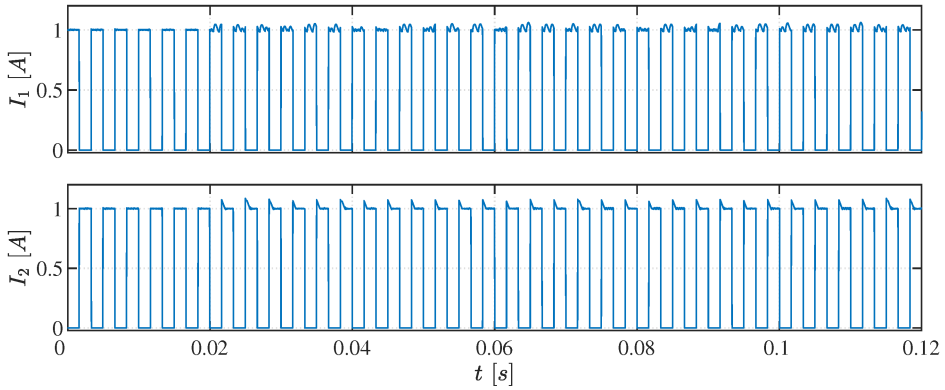


Fig. 7.7 Evolution of the string currents in the post-fault period, resulting from the deployment of a reconfiguration strategy in the SIMO converter. An OC fault takes place at t = 0.02 *s*.

The reconfiguration of the converter operation promotes important benefits, particularly for LED string 1, whose average current approaches the original value, reaching 0.5039 A.

7.2.2.2. Components stress

The stress imposed to the critical components of power converters is another criterion usually considered in the evaluation of the performance of power converters. Table 7.7 compares the stress imposed to the components of each converter architecture. The peak voltage and peak current imposed to the individual converter components are adopted as metrics to determine the stress imposed to the converter components.

TABLE 7.7 STRESS IMPOSED TO THE CONVERTER COMPONENTS

Parameter	SIMO Converter	Multiple Buck Converters
Switches voltage (V_{S_n})	V_{in}	V_{in}
Dimming switches voltage ($V_{S_{n\_LED}}$)	V_n	V_n
Diodes voltage (V_D)	V_{in}	V_{in}
Inductor(s) voltage (V_L)	V_{in} - V_n	V_{in} - V_n
Capacitors voltage (V_C)	V_n	V_n
Switches current (I_{S_n})	nI_n	I_n
Dimming switches current ($I_{S_{n\_LED}}$)	I_n	I_n
Diodes current (I_D)	I_n	I_n
Inductor(s) current (I_L)	nI_n	I_n
Capacitors current (I_C)	I_n	I_n

*__Nomenclature:__ n – number of converter channels/outputs

The evaluation of Table 7.7 reveals the similarity between the two architectures with regards to components stress. Exception to this statement is observed in the peak switches' current and peak inductor current. The switches with current control functions and the inductor of the SIMO converter are expected to be subjected to peak currents of n times the rated string current.

Being the power switches of a DC–DC converter susceptible to stress factors like overheating, it is important to develop a proper selection of these components. Particular attention should be therefore paid to the selection of the power switches deploying current control functions inside the SIMO converter, so that these components handle the expected peak current of n times the rated string current.

Also, it is worth noting that a proper selection of the inductor employed in the SIMO converter can effectively lower the peak currents experienced in the switches S_1 … S_n and in the inductor. The selection of an inductor with higher inductance will be fundamental to attain such goal.

7.2.2.3. Components count

The number of components required to build each LED driver architecture is defined through a generic count, based on the number of driver channels, denoted as n. Both active and passive components are considered in the computation of the total number of components. Table 7.8 establishes a comparison between the two topologies, in terms of components required to build a n-channel LED driver.

TABLE 7.8 COMPONENTS COUNT

Parameter	SIMO Converter	Multiple Buck Converters
Switches	$2n$	$2n$
Diodes	n	n
Inductors	1	n
Capacitors	$n + 1$	$n + 1$
Total no. of components	$4n + 2$	$5n + 1$

*__Nomenclature:__ n – number of converter channels/outputs

Based on the data of Table 7.8, it is stated that both configurations are pretty similar in terms of number of components, sharing the same number of switching devices, diodes, and capacitors. The difference between them lies on the number of inductors: while the SIMO converter employs a single inductor, the LED driver with multiple buck converters requires n inductors. Since inductors are particularly bulky and expensive components, the difference in the number of components makes the SIMO converter much more interesting with regards to volume.

It is worth noting that the analysis considers the implementation of multiple buck converters sharing a common DC-bus capacitor, inserted at the input of the LED driver, thus providing a simpler and effective power conversion solution. Alternatively, the inclusion of dedicated capacitors at the input of each buck converter could be considered as well, at the expense of a more complex and bulkier LED driver.

7.2.2.4. Cost effectiveness

To establish which converter architecture provides the most attractive solution with regards to cost of implementation, the evaluation developed herein compared the costs of acquisition of the components required to build each converter. Focus is put into the active and passive elements deemed critical to each converter; other minor components, common to the two converter architectures, are not included in this cost evaluation. The selection of the converters' components is based on the requirements of a four-channel LED driver, supplying four identical LED strings of 11 W each. On that basis, the following components have been considered for the cost analysis:

Multiple Buck Converters:

- *Main switches + diodes:* ALPHA & OMEGA SEMICONDUCTOR AOT12N40L, N-MOSFET; unipolar; 400V; 7A; 184W; TO220;
- *Dimming switches + diodes:* VISHAY IRF510PBF, N-MOSFET; unipolar; 100V; 4A; 43W; TO220AB
- *Diodes:* DIOTEC SEMICONDUCTOR MUR440L, 400V; 4A; DO201;
- *Inductors:* FERYSTER DTS-20/6,8/1,2-BV, 6.8mH, 1.2A, 100mΩ;
- *Capacitors:* Electrolytic Capacitor, Snap-in, 220 µF, 200 VDC + Electrolytic Capacitor, Snap-in, 220 µF, 400 VDC

Fault-Tolerant SIMO Converter:

- *Main switches + diodes:* ON SEMICONDUCTOR FQA30N40, N-MOSFET; unipolar; 400V; 30A; 290W; TO3PN;
- *Dimming switches + diodes:* VISHAY IRF510PBF, N-MOSFET; unipolar; 100V; 4A; 43W; TO220AB
- *Diodes:* DIOTEC SEMICONDUCTOR MUR440L, 400V; 4A; DO201;
- *Inductor:* FERYSTER DTS-31/6,8/5,0-V, 6.8mH, 5A, 30mΩ;
- *Capacitors:* Electrolytic Capacitor, Snap-in, 220 µF, 200 VDC + Electrolytic Capacitor, Snap-in, 220 µF, 400 VDC.

Table 7.9 provides a simplified estimation of the cost of ownership associated to each converter topology, developed with the abovementioned components. The presented estimation is based on a query to potential suppliers, carried out on the 23rd of August 2021.

TABLE 7.9 COST OF OWNERSHIP

Parameter	Multiple Buck Converters	SIMO Converter
Main switches + diodes	3.84 €	15.32 €
Dimming switches + diodes	1.64 €	1.64 €
Diodes	0.69 €	0.69 €
Inductor(s)	7.64 €	3.46 €
Capacitors	21.47 €	21.47 €
Total cost	35.28 €	42.58 €

Based on the data provided in Table 7.9, it is the LED lighting system based on multiple buck converters that represents the cheaper solution. For the conditions considered in the comparative analysis, the LED lighting system consisting of multiple buck converters costs 17.1 % less than the one based on the fault-tolerant SIMO converter. Such difference in the cost of the two solutions is justified by the distinctive technical specifications of the main switching devices required for each converter architecture.

Requiring switches with higher current ratings, the fault-tolerant SIMO converter involves a slightly higher cost of implementation. As for the remaining components, it is observed that there are very few differences among the two converter architectures in terms of cost. Most of the remaining active and passive components will have identical technical specifications for both converter architectures, making their cost of acquisition similar as well.

7.2.2.5. Conversion efficiency

One of the most critical performance metrics of any power conversion technology is precisely the power conversion efficiency. As for LED lighting applications, it is possible to define multiple metrics closely related to efficiency, that consider the electrical and/or optical performance of the system. In this study, focus is put into the LED driver and its electrical efficiency. Accordingly, the conversion efficiency is computed as follows:

$$\eta = \frac{\sum P_{1\ldots n}}{P_{in}} = \frac{P_1 + \ldots + P_n}{P_{in}} \tag{7.1}$$

where $P_1 \ldots P_n$ denotes the electrical power delivered to each LED string and P_{in} denotes the electrical power measured at the input of the LED driver.

The power delivered to each LED string $P_1 \ldots P_n$ depends not only on the string voltage and current, but also on the dimming period, and is computed as follows:

$$P_n = \frac{1}{T_{\text{dim}}} \int_0^{T_{\text{dim}}} V_n \times I_n \tag{7.2}$$

where T_{dim} refers to the dimming period, V_n denotes the nominal LED string voltage, and I_n denotes the nominal LED string current.

To assist on the determination of the efficiency, the simulation model of each converter architecture has been adopted as the source of results. The parameters employed in the simulations of the four-channel LED drivers are listed in Table 7.5 and Table 7.6.

Fig. 7.8 depicts the efficiency maps that establish a relation between the dimming ratio, the rated string current, and the power conversion efficiency, for LED drivers based on the converter topologies under evaluation.

The results reveal that the trend of evolution of the efficiency over the pair 'rated string current – dimming' is common to both architectures. Overall, the SIMO converter provides a broader region of operation with efficiency surpassing 90 %. Also, the SIMO converter provides fairly higher efficiency within the low-power region. At low dimming, low rated string current, the efficiency gains reach up to 10 %.

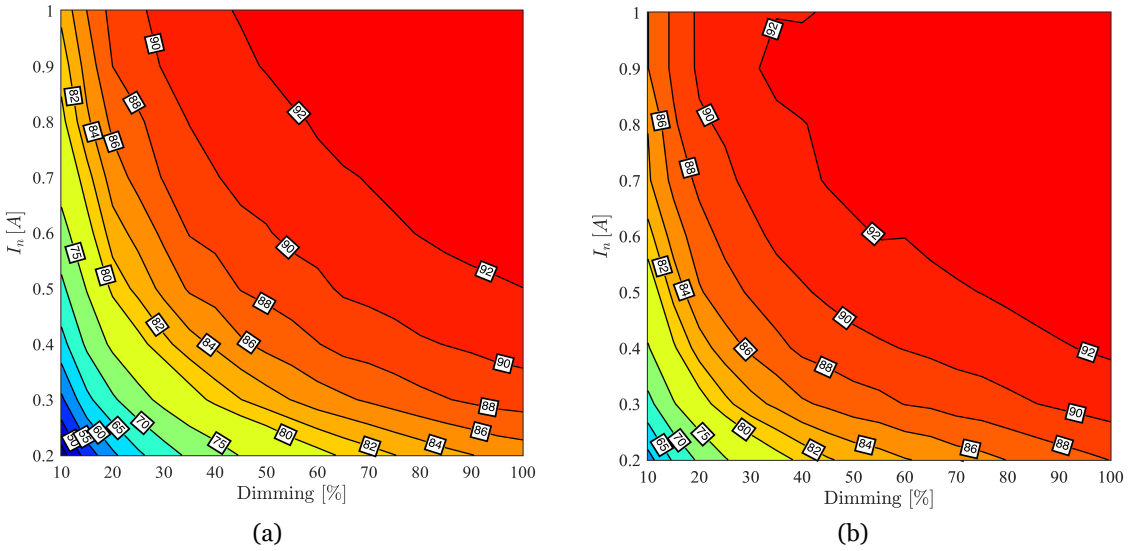


Fig. 7.8 Efficiency maps related to the four-channel configurations of the LED drivers under evaluation: (a) multiple buck converters; (b) SIMO converter.

The general advantage of the SIMO converter in terms of efficiency is explained by the lower number of components and consequent reduction in the switching/conduction system increases, since the difference between the two architectures in terms of number of components should also increase.

7.2.3. Analysis of results

The comparative evaluation of the two LED driver architectures reveals the importance of developing a multi-parametric evaluation of the performance of power conversion systems targeted at lighting applications.

Based on the performance analysis presented previously, it is possible to take some important conclusions.

The fault-tolerant SIMO LED driver appears as the most promising solution to assure continuous power supply to multiple LED strings, even in case of failure of the converter semiconductors. The inherently fault tolerant architecture of the converter enables continuous supply of energy to all LED strings, even without deploying any reconfiguration measures. Naturally, the response of the system will not be optimal, as part of the lighting system will provide less luminous flux. Through the adoption of proper reconfiguration measures, free of any additional hardware, it becomes possible to recover most of the original lighting conditions in all LED strings, with minimal impact on the quality of the light being produced.

The SIMO converter also provides an important advantage over the conventional solution, employing multiple buck converters, in terms of power conversion efficiency and number of components. Particularly, the reduced number of passive components required

to build the SIMO converter provide an appealing and significant advantage in terms of volume.

The only criteria where the solution based on multiple buck converters gains advantage lies on the cost of ownership and on the stress imposed to the individual components of the converter. Two parameters dictate such advantage: the peak switch current and the peak inductor current.

In conclusion, a global evaluation and weighting of the performance criteria allows to state that the LED lighting system based on the fault-tolerant SIMO converter has potential to become as the most appealing and interesting solution for DC-supplied residential LED lighting systems with high availability and efficiency.

Chapter 8

Conclusions and Future Works

8.1. Conclusions

This thesis provided an investigation on fault-tolerant DC–DC converters, suitable for DC microgrids deployed in the context of homes and offices. Strategies for improving the efficiency and, most importantly, the availability of such converters were presented and evaluated.

Until very recently, DC–DC converters were mainly employed in niche applications, typically involving fairly low power ratings. These converters may soon become part of office equipment and home appliances, due to the increasing concerns about energy efficiency and optimisation of resources in businesses and residences. Offices' equipment and home appliances require power converters with high reliability levels, in order to extend their lifespan. DC–DC converters, like any other converter, may suffer faults that degrade their smooth operation, compromising the converters themselves as well as the load(s) connected to them, thus reducing the lifespan of the entire group (converter + load). Locating the faulty element to take remedial actions that minimise harmful consequences presents, therefore, pivotal relevance.

At a first stage of this thesis, attention was devoted to the study and modelling of the end-uses to supply resorting to DC–DC converters. Taking profit from the knowledge and techniques available in the scientific literature, analytical models were derived for LED lighting and EV charging applications, to understand their electrical behaviour and simulate their operation.

Based on the evaluation of a set of requirements strictly related to each end-use, non-isolated DC–DC converters capable of better fulfilling such requirements were selected. Five distinctive converter topologies have been selected, targeting the three major categories of end-uses (general appliances, LED lighting and EV charging). For each converter topology, the adopted control strategies have been briefly described. Along with the converter requirements themselves, the selected control strategies also considered the set of requirements posed by each end-use.

Then, the response of the selected DC–DC converter topologies under healthy and faulty conditions was thoroughly evaluated, based on the monitorisation of electrical

variables strictly related to the converter. Such evaluation focused particular attention on two topologies: the non-isolated unidirectional interleaved boost converter and the fault-tolerant SIMO converter. The evaluation of these two topologies is justified by the fact that both sustain part of their power conversion capabilities, even in the presence of OC faults on the power switches. Naturally, the fault condition negatively impacts parameters like the amplitude and frequency of the current ripple (for the non-isolated unidirectional interleaved boost converter) or the amplitude of the converter output current (for the fault-tolerant SIMO converter).

The information extracted from the developed fault analysis was then used to propose a novel fault diagnostic strategy for interleaved converters. The strategy relies on the observation of the converter input current at precise instants, without requiring the development of complex mathematical computations or emulation of the converter model. The advantages of the proposed fault diagnostic strategy in comparison to the state-of-the-art are twofold: 1) effective diagnostic of faults is attained for a significant range of operation points; 2) fast diagnostic is achieved, thanks to the simplicity of the proposed strategy. Such features make the fault diagnostic algorithm way more suitable for DC applications framed in homes and offices, if compared to similar solutions of the state-of-the-art.

With regards to fault tolerance, a very comprehensive set of solutions was presented.

For the non-isolated unidirectional interleaved boost converter targeted at general appliances, a hybrid reconfiguration approach, consisting of the combination of phase-shift correction and variable frequency operation. Phase-shift correction was the most common reconfiguration strategy used in previous works focused on fault tolerance of interleaved converters. On the other hand, variable frequency gate drivers proposed in the literature were mainly focused on other purposes than the fault tolerance. This work showed that both phase-shift correction and variable frequency operation are effective when applied in interleaved converters. Besides, it was shown that the combination of several reconfiguration techniques leads to improved results, not achieved in fault-tolerant converters that make use of a single reconfiguration strategy. Great benefits are attained in the operation of faulty DC–DC converters, enabling the continued operation of the converter, without resorting to any redundant components. Concurrently, important performance metrics, like the conversion efficiency or the current ripple, are successfully kept for the post-fault operation.

For LED lighting applications, a novel fault-tolerant LED driver architecture was presented. Indeed, the proposed fault-tolerant LED driver is the only solution available in the literature capable of ensuring the continuous operation, under degraded mode, of all LED strings after OC faults in the switches with current control functions. To improve the response of the fault-tolerant SIMO converter over the post-fault period, two distinctive

reconfiguration approaches were proposed. They ensure that none of the LED strings suffer significant depreciation of luminous flux when any of the switches with current control functions fails. Experimental results revealed that the implementation of the reconfiguration strategies successfully recovers the average current flowing through the LED string(s) connected to the faulty driver channel(s). In practice, such achievement translates into a significant restoration of the luminous flux produced by LED string(s) connected to faulty channel(s) of the LED driver. In addition, the adoption of the reconfiguration strategies revealed promising results in the sense of overcoming the negative consequences of LED lighting systems containing parasitic components typically associated to long cabling. Finally, a sensorless current control strategy was presented. As it obviates the requirement of individual current control loops to monitor each of the LED strings connected to a single LED driver, the proposed current control strategy provides an effective solution for the improvement of the LED driver reliability. Losses incurred by the current sensing resistors are obviated, as one of the most important sources of heat generation elements is removed from the circuit.

Finally, comparisons were established between candidate DC–DC converter topologies for DC microgrids deployed at homes and offices. With respect to LED lighting applications, the fault-tolerant SIMO converter reveals advantage over the solution based on multiple buck converters in terms of fault tolerance, cost of implementation and efficiency. As for EV charging applications, it is concluded that both topologies provide interesting merits. In case that preference is given to cost effectiveness, conversion efficiency, and fault tolerance, the interleaved converter should be seriously considered as the topology of preference. On the other hand, the multilevel converter appears to be the most suitable solution for the development of EV chargers featuring reduced voltage stress and improved efficiency at low-power charging.

8.2. Future Works

As a result of this work, very fruitful developments were introduced in the sense of better understanding district-scale DC microgrids and related power conversion solutions. Still, it became quite evident that the developments and achievements attained in the framework of this work were not able to properly cover the entire range of appliances commonly found at homes and offices and, as a result, to evaluate all DC–DC converters considered relevant in this domain. For that reason, it is important to promote further developments on fault diagnosis and fault tolerance of other key DC–DC converter topologies, suitable for homes and offices. The evaluation made to the state-of-the-art suggests that there is room for improvements on fault diagnosis and fault tolerance of converter topologies integrating galvanic isolation. These converter topologies reveal

particular interest, for instance, to supply sensitive appliances, like computers, TVs or related electronics.

Fault prognosis is a recent and emerging field of research that seeks for improvements on the availability of power electronics. Developing novel fault prognostic strategies, targeted at DC–DC converter topologies for homes and offices, also ascertains as a promising research topic for future works.

Given the multitude of elements integrated on district-scale DC microgrids, this work focused on some of the most promising DC–DC converter topologies for interfacing DC microgrids with energy storage elements and with loads. Still, it is also of interest to evaluate the performance and to introduce developments on the availability of converter topologies for interfacing DC microgrids with microgeneration technologies (wind turbines, photovoltaic systems, and fuel cells).

This work provided a generic and simple evaluation of the most representative DC–DC converter topologies, when operated under healthy condition. Still, it is relevant to develop a broader and deeper performance evaluation of the entire range of DC–DC converter topologies deemed suitable for homes and offices, considering aspects like the thermal performance or the efficiency, assessed also in case of degraded converter operation.

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Appendix A

Computational Simulation Models

This appendix provides information regarding the parameters considered in the multiple simulation models developed in the framework of this thesis.

A.1. Non-isolated unidirectional interleaved boost converter

To confirm the theoretical formulation developed for the non-isolated unidirectional interleaved boost converter, a simulation model was established using *Simulink™*. The main parameters adopted in the simulation model are summarised in Table A.1. The converter output voltage V_{out} is varied over a comprehensive range of values, in order to address a wide range of variation of the duty cycle D.

TABLE A.1 PARAMETERS OF THE NON-ISOLATED UNIDIRECTIONAL INTERLEAVED BOOST CONVERTER

Parameter	Nomenclature	Value
Input Voltage	V_{in}	24 V
Inductance	L_i	7.6 mH
Output capacitance	C_{out}	680 μF
Load resistance	R_o	30 Ω
Switching frequency	f_{sw}	{1, 3 , 5} kHz
Simulation sampling time	T_s	5 μs

A.2. Fault-tolerant SIMO converter

The simulation model of the fault-tolerant LED lighting system, also implemented in *Simulink™*, is comprised of the converter, represented in Fig. 3.5, and the corresponding controller, represented in Fig. 3.6. The structure of the controller is modular, meaning that it has to be replicated according to the number of channels/outputs of the LED driver. Table A.2 summarises the parameters employed in the simulation model developed for the fault-tolerant LED lighting system.

TABLE A.2 PARAMETERS OF THE FAULT-TOLERANT SIMO CONVERTER

Parameter	Nomenclature	Value
Input Voltage	V_{in}	{120, 200} V
Inductance	L	4 mH
Capacitance	C	200 μF
Current sensing resistance	$Rs_{1...n}$	2 Ω
No. of LED strings	n	2, 4
LED string nominal voltage	$V_{n_{nom}}$	48 V
LED string nominal current	$I_{n_{nom}}$	0.22 A
LED string nominal power	$P_{n_{nom}}$	11 W
Switching frequency (time-sharing function)	f_t	{2, 10} kHz
Dimming frequency	f_{dim}	{300, 500} Hz
Simulation sampling time	T_s	10 μs

A.3. Fault-tolerant SIMO converter integrating cable parasitics components

The architecture of the LED lighting system comprising cabling parasitics is identical to the one of the LED lighting system neglecting the parasitic components. Apart the parasitic components, parameters like the converter inductance or the switching frequency are also varied. Table A.3 lists the most relevant parameters adopted in the model.

TABLE A.3 PARAMETERS OF THE FAULT-TOLERANT SIMO CONVERTER INTEGRATING CABLING PARASITICS

Parameter	Nomenclature	Value
Input voltage	V_{in}	120 V
Inductance	L	7.6 mH
Capacitance	$C_{1...n}$	200 μF
Current sensing resistance	$Rs_{1...n}$	2 Ω
Cable resistance	R_p	2 Ω
Cable inductance	L_p	2.5 mH
No. of LED strings	n	2
LED string nominal voltage	$V_{n_{nom}}$	48 V
LED string nominal current	$I_{n_{nom}}$	0.22 A
LED string nominal power	$P_{n_{nom}}$	11 W
Switching frequency (time multiplexing function)	f_t	5 kHz
Dimming frequency	f_{dim}	{300, 1000} Hz
Simulation sampling time	T_s	10 μs

A.4. Sensorless current control of the fault-tolerant SIMO converter

To validate the resiliency and effectiveness of the sensorless current control strategy, a simulation model was developed in *Simulink™* environment. Table A.4 compiles the most relevant information about the parameters employed in the simulation model.

TABLE A.4 PARAMETERS OF THE FAULT-TOLERANT SIMO CONVERTER USED TO EVALUATE SENSORLESS CURRENT CONTROL

Parameter	Nomenclature	Value
Input voltage	V_{in}	300 V
Inductance	L	2 mH
Capacitance	$C_{1...n}$	200 μF
No. of LEDs per string	m	10
No. of LED strings	n	3
LED string nominal voltage	$V_{n_{nom}}$	48 V
LED string nominal current	$I_{n_{nom}}$	0.22 A
LED string nominal power	$P_{n_{nom}}$	11 W
Switching frequency (time multiplexing function)	f_t	50 kHz
Dimming frequency	f_{dim}	300 Hz
Simulation sampling time	T_s	10 μs

Appendix B

Experimental Setups

This appendix describes the processes of implementation of the laboratory prototypes developed to evaluate the power conversion architectures considered in this thesis.

B.1. Non-isolated unidirectional interleaved boost converter

The non-isolated unidirectional interleaved boost converter was considered as the power conversion architecture compatible with the requirements of general appliances. To validate the proposed strategies, a prototype of the non-isolated unidirectional interleaved boost converter was connected to a DC supply, obtained from a three-phase rectified power supply (see Fig. B.1). The input voltage is regulated through an auto-transformer. To obtain a stable voltage from the rectifier output, a bank of capacitors is connected in parallel with

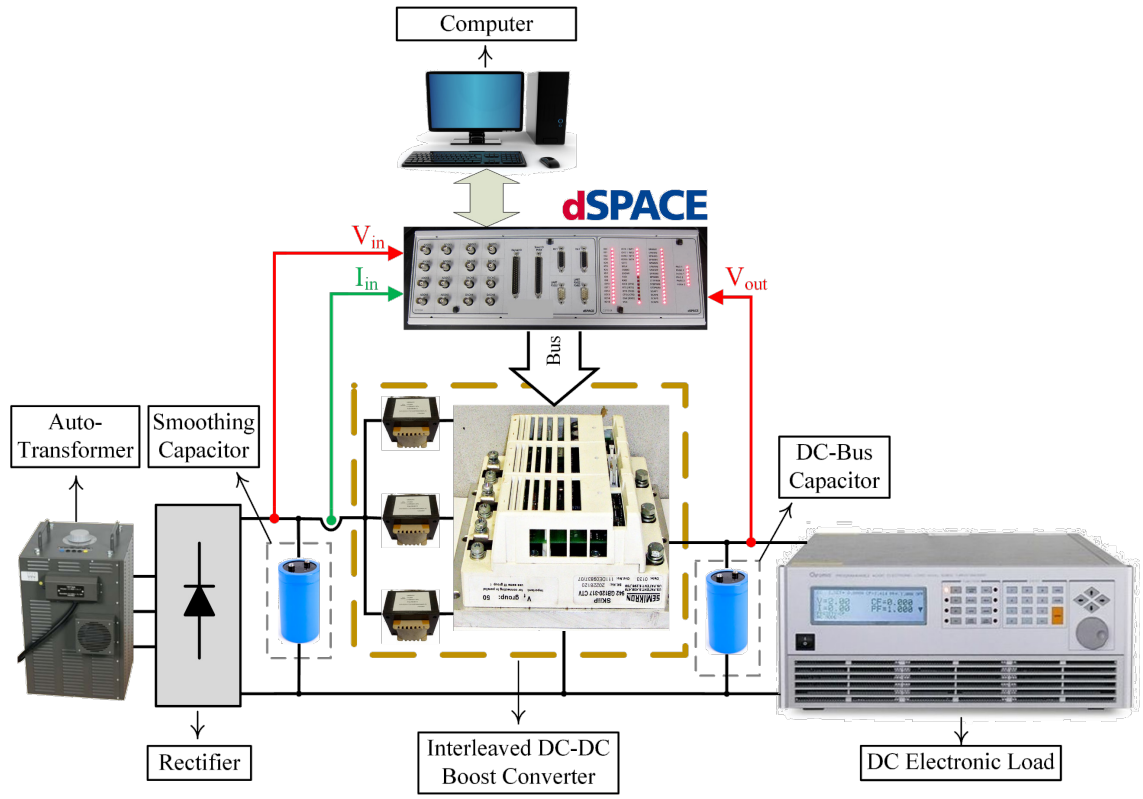

Fig. B.1 Schematic of the experimental assembly considered in the laboratory tests of the non-isolated unidirectional interleaved boost converter.

the rectifier output. A programable electronic load serves as sink of the converter output power, operating under constant resistance condition, to emulate a 30 Ω resistor.

Only the converter input current I_{in}, input voltage V_{in}, and output voltage V_{out} signals are introduced in the DSP. These variables are measured for both control and operation monitoring purposes. The DSP consists of a dSPACE DS1103, and is responsible for acquiring input variables, deploy the control actions, and generate the PWM command signals to send to the power converter. The digital controller operates with a sampling time of 20 μs. To force an OC fault in any of the converter IGBTs, the desired PWM signal(s) are turned off using the dSPACE ControlDesk software.

Table B.1 lists the parameters of the elements employed in the experimental assembly, whose schematic representation is provided in Fig. B.1.

TABLE B.1 PARAMETERS OF THE NON-ISOLATED UNIDIRECTIONAL INTERLEAVED BOOST CONVERTER IMPLEMENTED IN LABORATORY

Parameter	Nomenclature	Value
Input voltage	V_{in}	23-26 V
Phase inductance	$L_{1...n}$	7.6 mH
Input capacitance	C_{in}	8800 μF
Output capacitance	C_{out}	680 μF
Load resistance	R_{out}	30 Ω
Switching frequency	f_{sw}	{1, 3, 5} kHz
Controller sampling time	T_s	20 μs

B.2. Fault-tolerant SIMO converter

The prototype of the fault-tolerant SIMO buck converter, considered in this thesis as the elective power conversion architecture for supplying LED loads, employs part of the components considered for the unidirectional interleaved boost converter, described in Section B.1. The DC supply is obtained from a three-phase rectified power supply with smoothing capacitor (see Fig. B.2). The input voltage is regulated through the auto-transformer.

Each converter output supplies one LED string. The number of converter outputs equals the number of LED strings.

As observed in Fig. B.2, the DSP collects data from the converter input current I_{in}, input voltage V_{in} and voltages of the two current sensing resistors ($V_{R_{S\_1}}$ and $V_{R_{S\_2}}$). While voltages $V_{R_{S\_1}}$ and $V_{R_{S\_2}}$ are monitored for both control and operation monitoring purposes, I_{in} and V_{in} are solely monitored for operation monitoring purposes.

The DSP consists of a dSPACE DS1103 controller, and is responsible for acquiring variables, deploying the control actions, and generating the gating signals to send to the power converter. The digital controller operates with a sampling time of 25 μs.

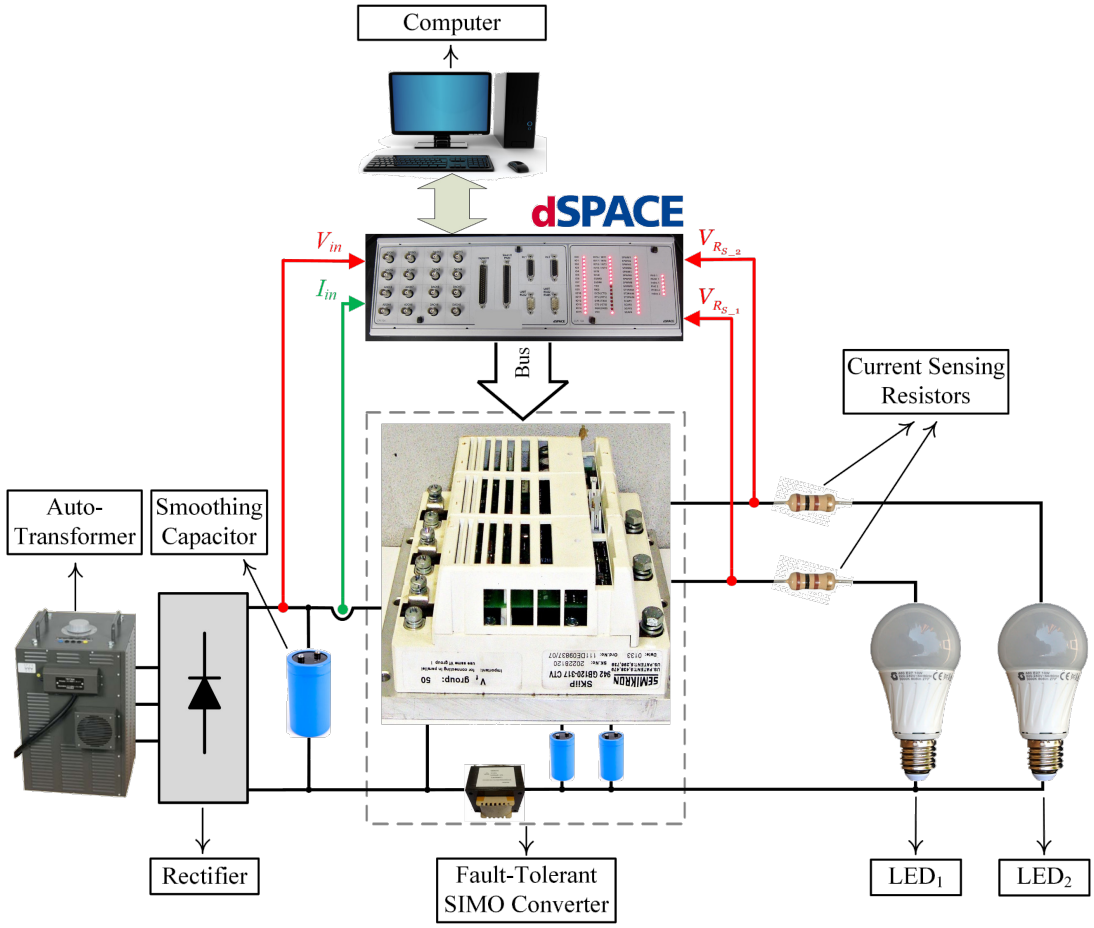

Fig. B.2 Schematic of the experimental assembly used to test the fault-tolerant SIMO converter.

Table B.2 lists the parameters of the elements employed in the experimental assembly, whose schematic representation is provided in Fig. B.2.

TABLE B.2 PARAMETERS OF THE FAULT-TOLERANT SIMO CONVERTER IMPLEMENTED IN LABORATORY

Parameter	Nomenclature	Value
Input voltage	V_{in}	120 V
Inductance	L	4 mH
Capacitance	$C_{1\ldots n}$	200 μF
Current sensing resistance	$Rs_{1\ldots n}$	2 Ω
No. of LED strings	n	2
LED string nominal voltage	$V_{n_{nom}}$	48 V
LED string nominal current	$I_{n_{nom}}$	0.22 A
LED string nominal power	$P_{n_{nom}}$	11 W
Time-sharing frequency	f_t	2 kHz
Dimming frequency	f_{dim}	300 Hz
Controller sampling time	T_s	25 μs

B.3. Fault-tolerant SIMO converter integrating cable parasitics components

The evaluation of the fault-tolerant SIMO converter in the presence of cable parasitics components is supported experimentally through a laboratory prototype with physical structure identical to the one described in Section B.2. Fig. B.3 provides a schematic representation of the laboratory prototype implemented to test the fault-tolerant SIMO converter in the presence of cable parasitics components.

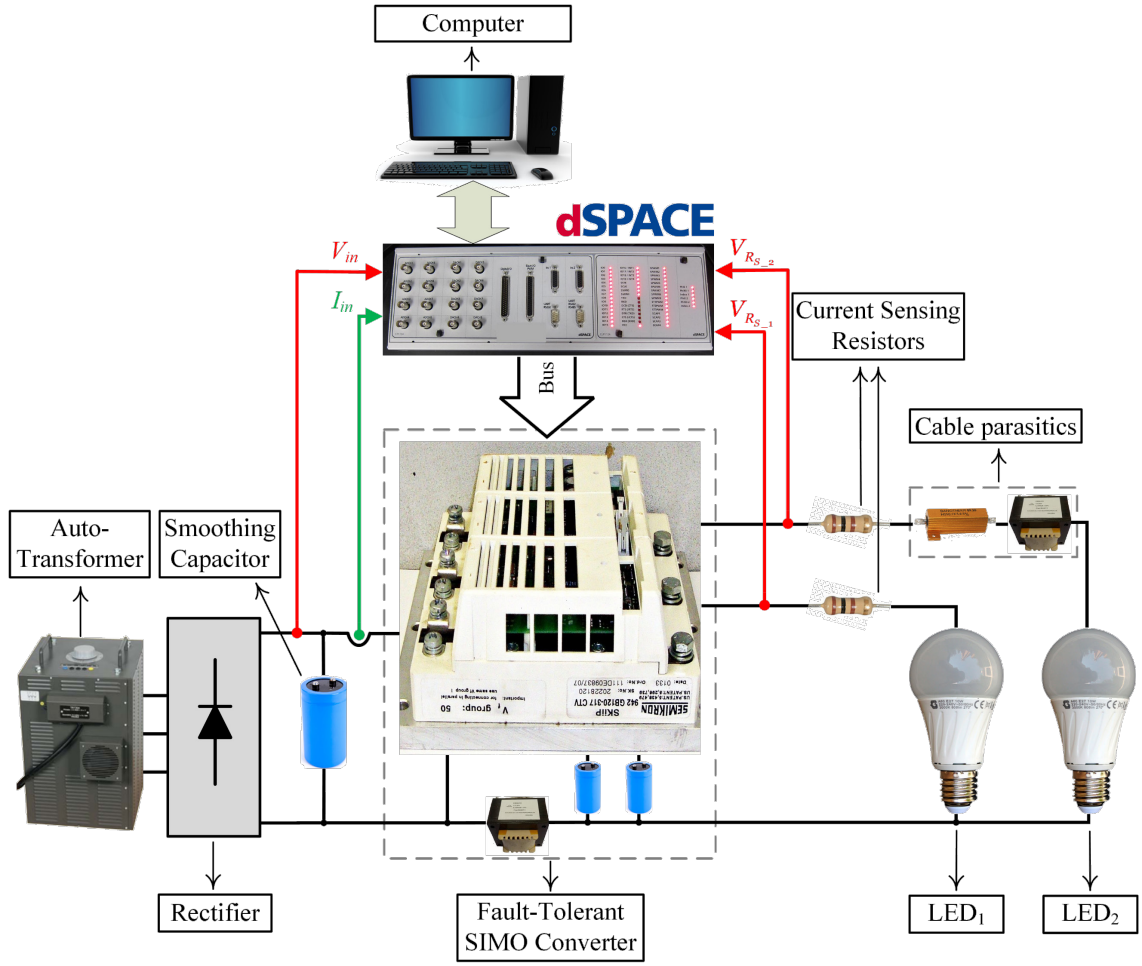

Fig. B.3 Schematic of the experimental assembly adopted to test the fault-tolerant SIMO converter integrating cable parasitics components.

Cable parasitics are introduced in only one of the outputs of the SIMO converter. Such parasitics are emulated resorting to a resistor and an inductor.

Table B.3 lists the parameters of the elements employed in the experimental assembly, whose schematic representation is provided in Fig. B.3.

TABLE B.3 PARAMETERS OF THE FAULT-TOLERANT SIMO CONVERTER INTEGRATING CABLE PARASITICS COMPONENTS

Parameter	Nomenclature	Value
Input voltage	V_{in}	120 V
Inductance	L	7.6 mH
Capacitance	$C_{1\ldots n}$	200 μF
Current sensing resistance	$Rs_{1\ldots n}$	2 Ω
Cable resistance	R_p	2 Ω
Cable inductance	L_p	2.5 mH
No. of LED strings	n	2
LED string nominal voltage	$V_{n_{nom}}$	48 V
LED string nominal current	$I_{n_{nom}}$	0.22 A
LED string nominal power	$P_{n_{nom}}$	11 W
Switching frequency (time multiplexing function)	f_t	5 kHz
Dimming frequency	f_{dim}	300 Hz
Controller sampling time	T_s	25 μs